NANOMAGNETISM FOR ICT:

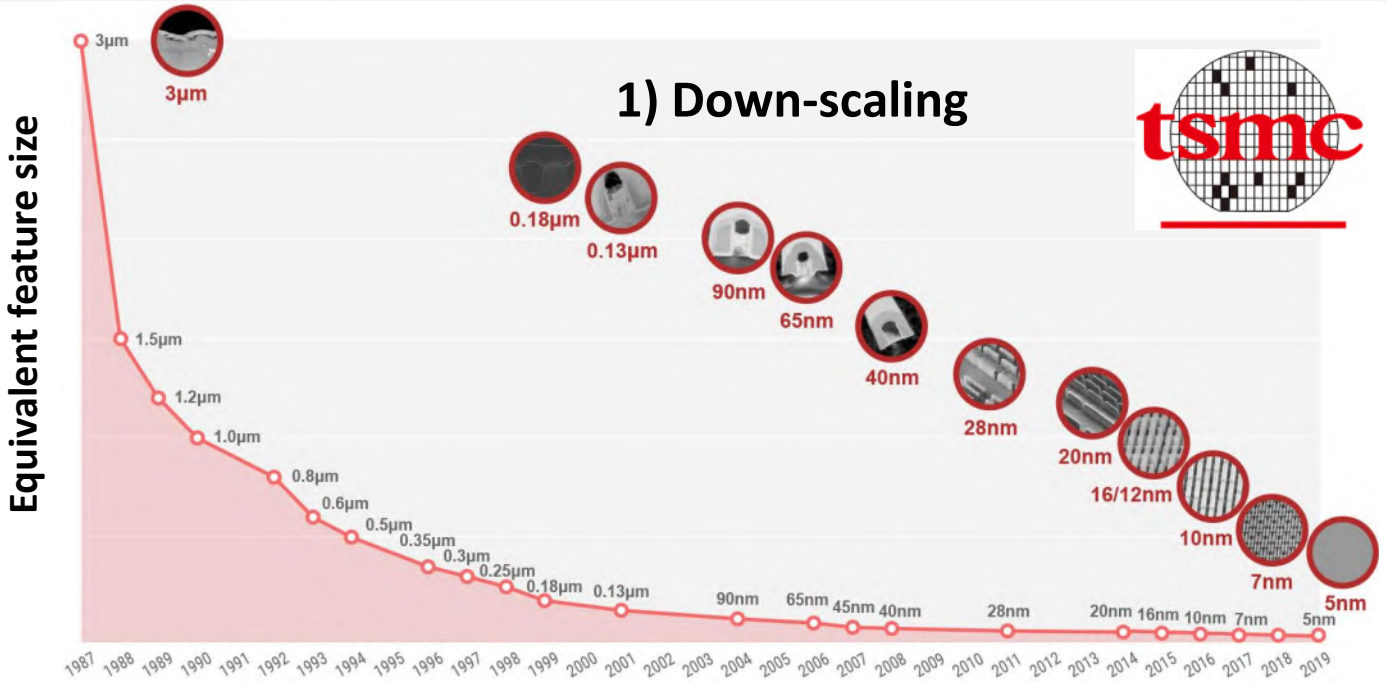
FROM SPINTRONICS TO NEUROMORPHIC

B.Dieny

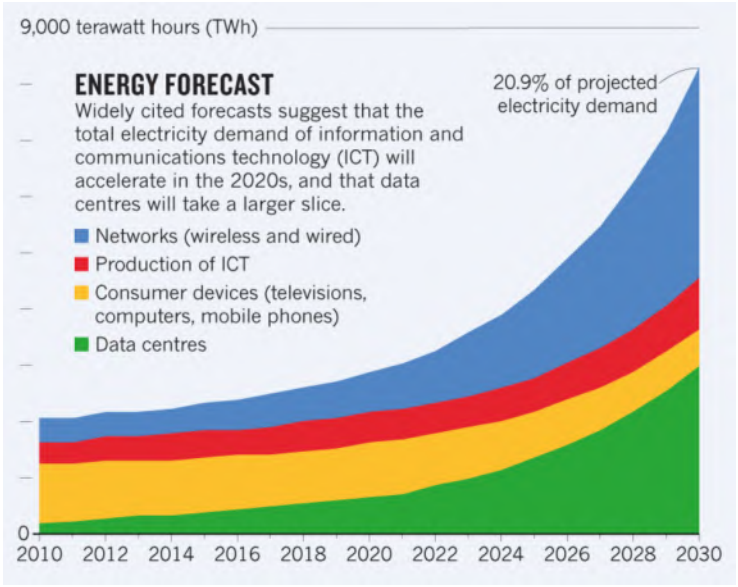
Acknowledgements: O. Fruchart

General trends in microelectronics

1) Down-scaling

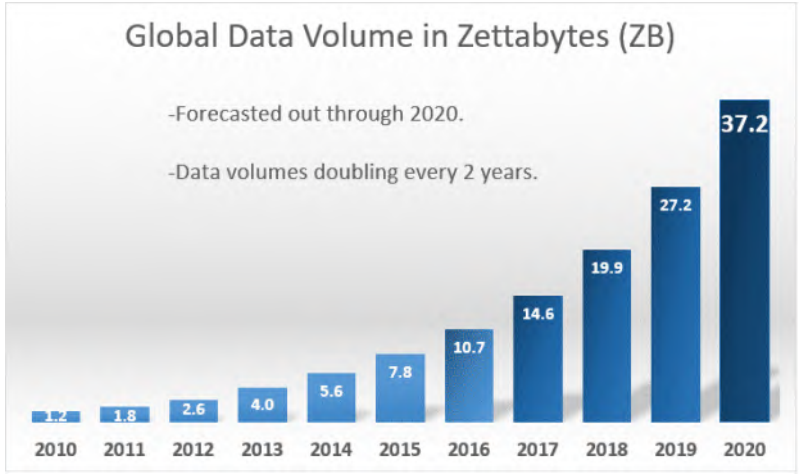


2) Power consumption



Nicola Jones, https://www.nature.com/articles/d41586-018-06610-y

3) Volume of data



These trends yield to physical limits : New paradigms are needed (Beyond CMOS).

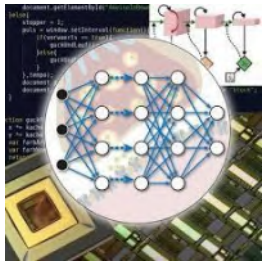
Spintronics can help !

Spin-electronics can help !

- Data storage thanks to steadily increasing areal density on hard disk drives

- Non-volatile magnetic memories (MRAM) to reduce power consumption and speed up communication between logic and memory

- Neuromorphic architecture to improve computing efficiency for specific applications



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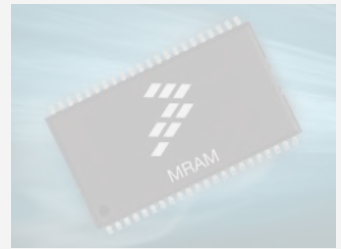
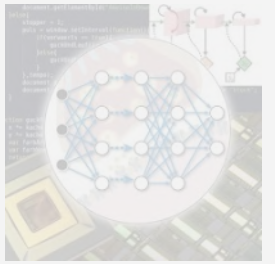
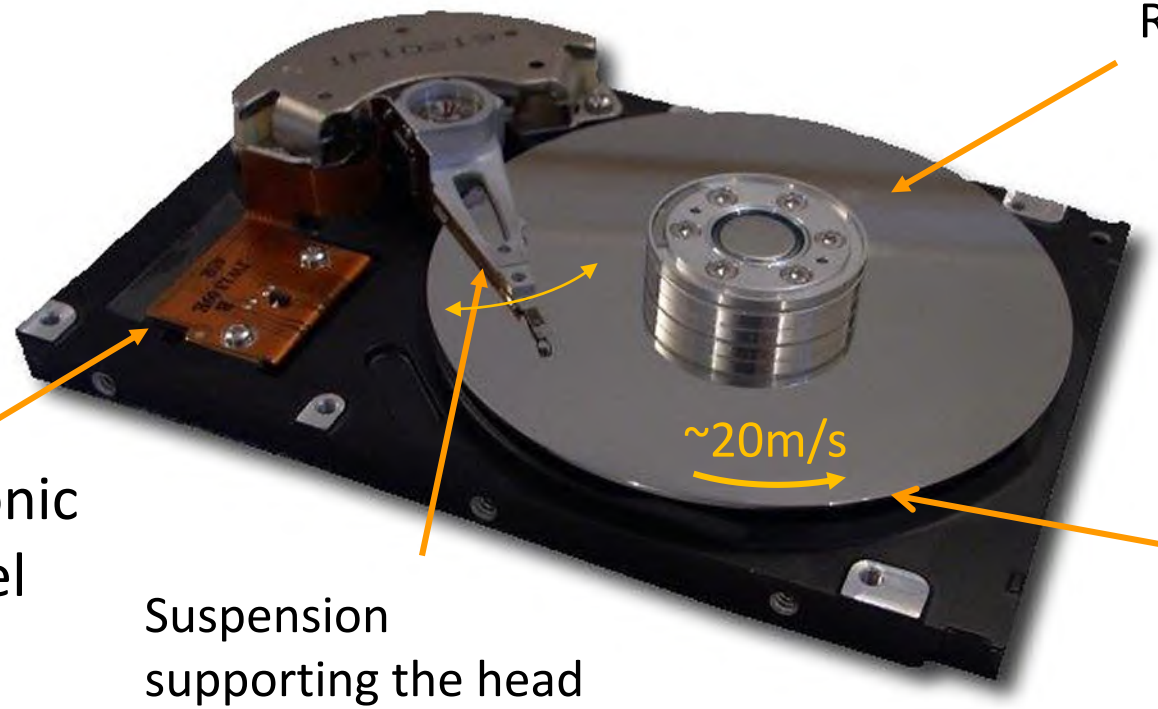


- Neuromorphic architecture to improve computing efficiency for specific applications



Inside a hard disk drive

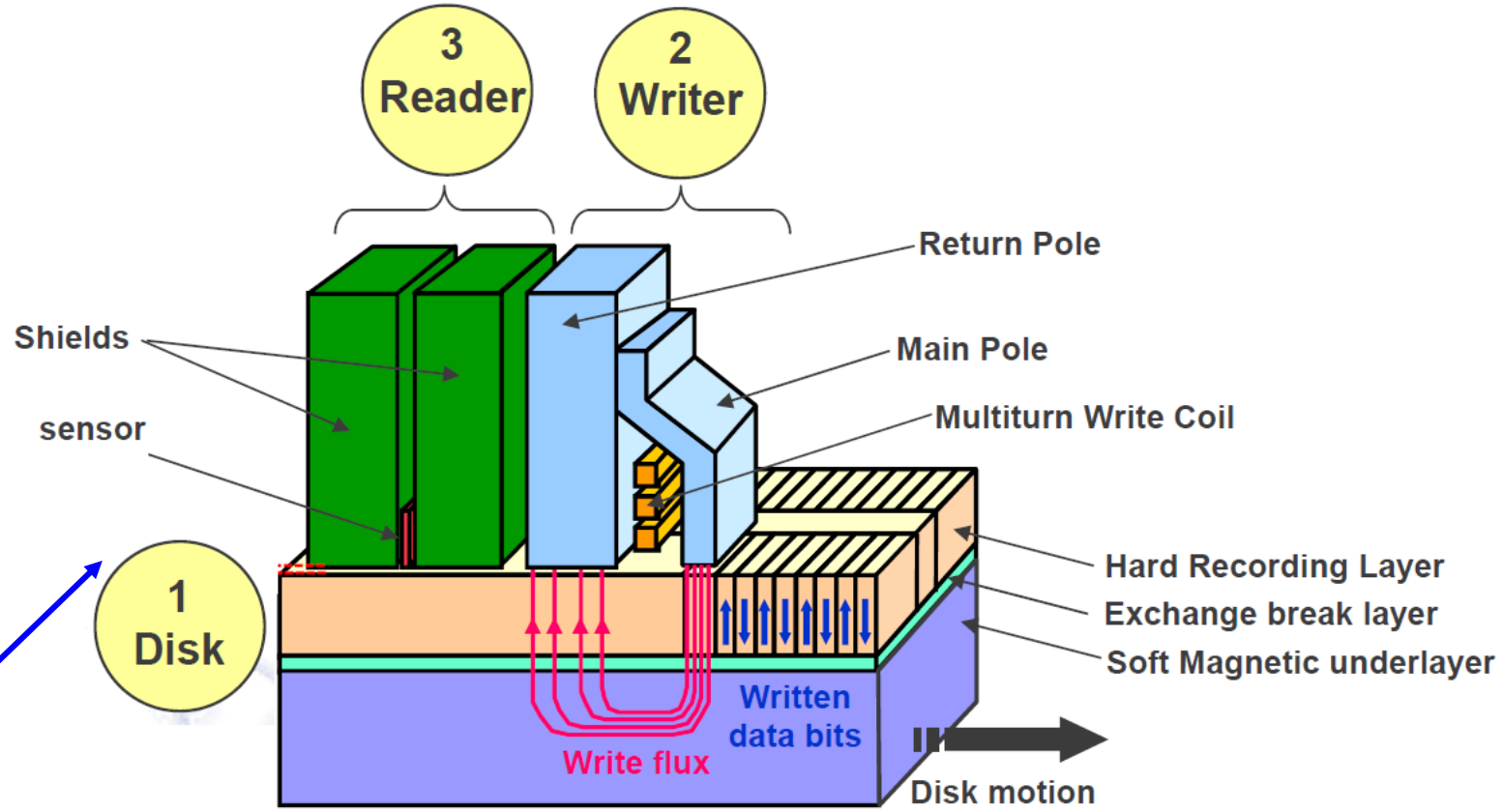
In most HDD, several disks are stacked (up to 10 nowadays) with one head per plate



Areal density used to increase by 60%/year but access time decreased by only ~5% per year

Principle of magnetic recording

Hard Disk Drive (HDD)



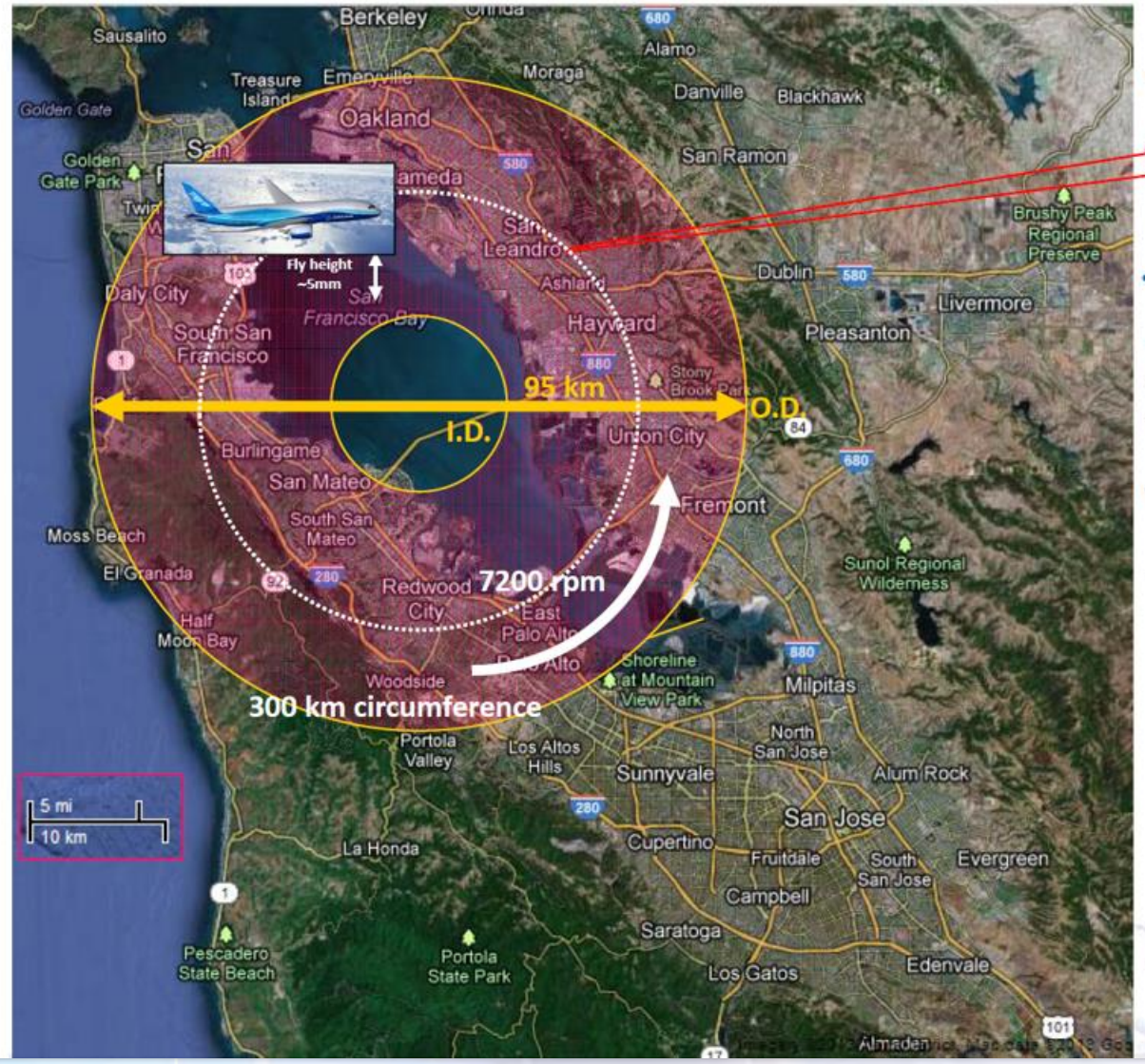
GMR spin-valve heads from 1998 to 2004, TMR heads since 2004

Present areal density ~1Tbit/in² = 155 Gbit/cm²
Bit size ~ 20 nm x 40nm
Disk rotating at 7000-10000rpm, linear velocity of ~20m/s
Head fly height ~ 5nm

HDD: a « Formule 1+++ » Technology

Thanks to J.Childress

Today's 700Gb/in² HDD technology ---- Scaled × 1 million



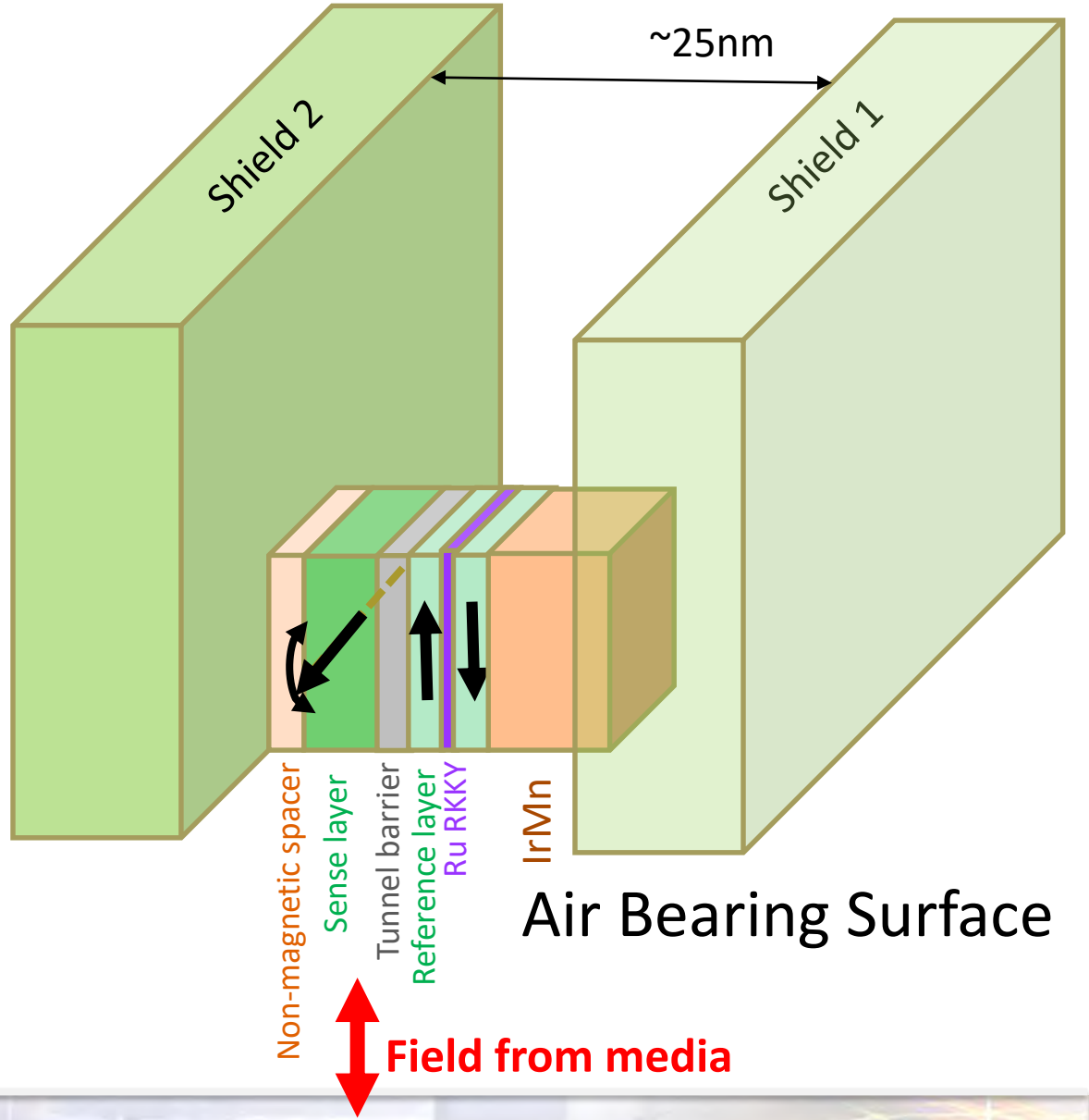
- Media Disk = SF Bay Area (95 km dia)
- 1bit = 1 finger (1.5 × 8cm)
- Read/Write Head = Passenger jet airplane
- Fly speed @ O.D.
  = 7200 rpm × 300 km
  = 0.12 c (c=3x10⁸m/s speed of light)
- Fly height = 5mm

HDD × 1 million =

" A passenger jet airplane
-- flying at 12% of the speed of light
– only 5mm above the ground
-- around the SF Bay area
– all the while seeking, reading and writing bits of information the size of a finger"

MR sensors for magnetoresistive heads

- Heads based on MgO based magnetic tunnel junctions
- Typical sensor size ~ 30nm x 30nm
- Sensor resistance ~ a few hundred Ω to match pre-amplifier input impedance
- Implies very low RA magnetic tunnel junctions (below 1Ω.μm²)
- TMR as large as possible but typically ~50% for RA~0.5Ω.μm²
- Steady need to reduce RA, increase MR amplitude, decrease shield to shield spacing
- New schemes needed to keep on increasing areal density (CPP-GMR with Heusler alloys, lateral spin-valves…)



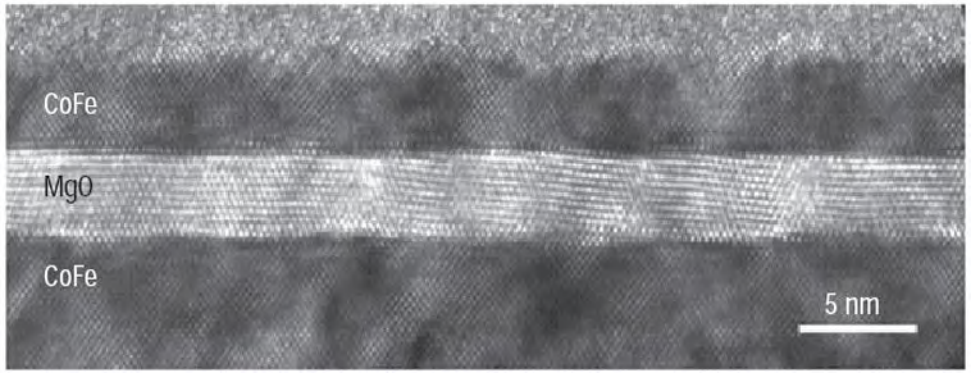
Giant TMR of MgO tunnel barriers

S.S.P.Parkin et al, Nature Mat. (2004), nmat1256.

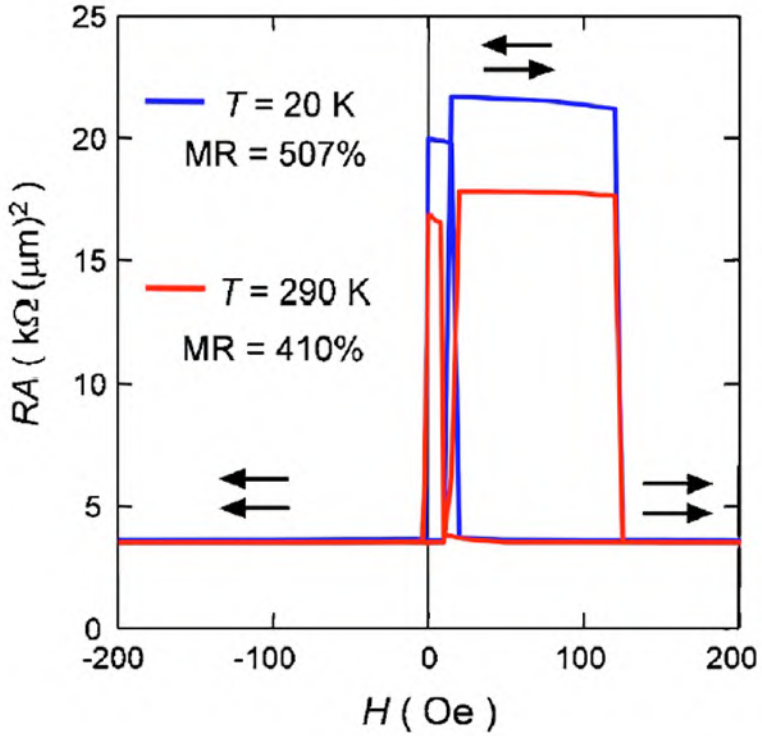
S.Yuasa et al, Nature Mat. (2004), nmat 1257.

- Very well textured MgO barriers grown by sputtering or MBE on bcc CoFe or Fe magnetic electrodes, or on amorphous CoFeB electrodes followed by annealing to recrystallize the electrode.
- High TMR due to additional spin-filtering effect associated with symmetry of electron wave functions.

Yuasa et al, APL89, 042505(2006)



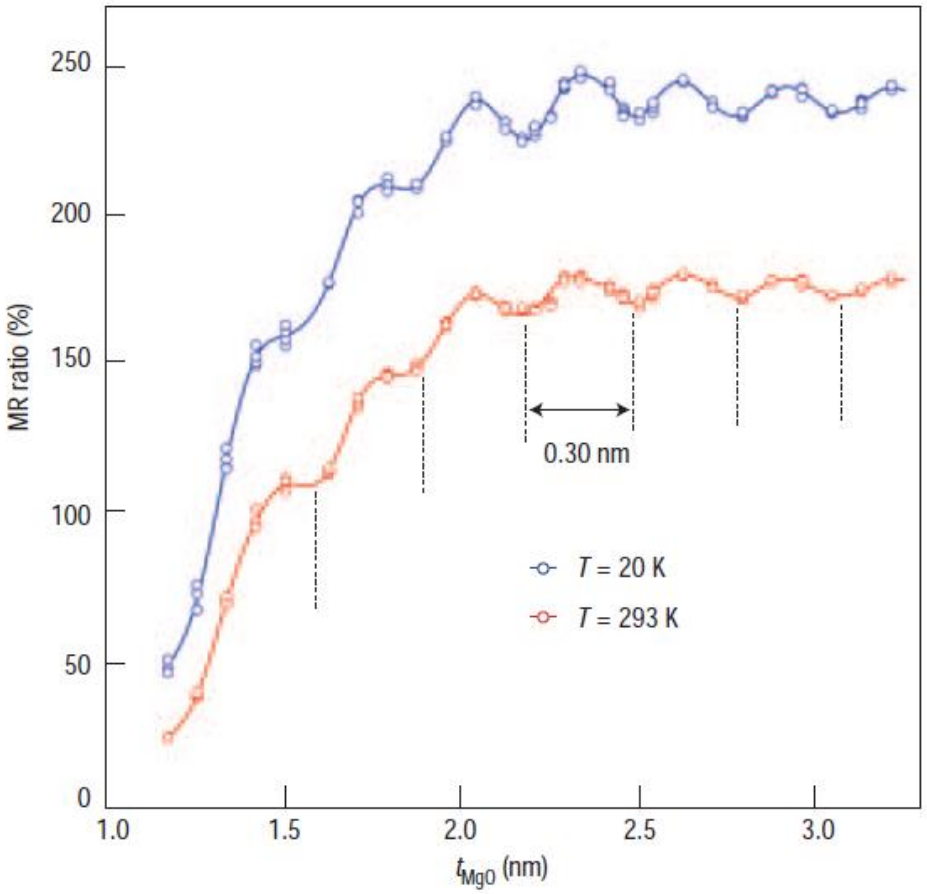
Au cap 50 nm
Ir-Mn 10 nm
Fe(001) 10 nm
Co(001) 0.57 nm
MgO(001) 2.2 nm
Co(001) 0.57 nm
Fe(001) 100 nm
MgO(001) 20 nm
MgO(001) sub.



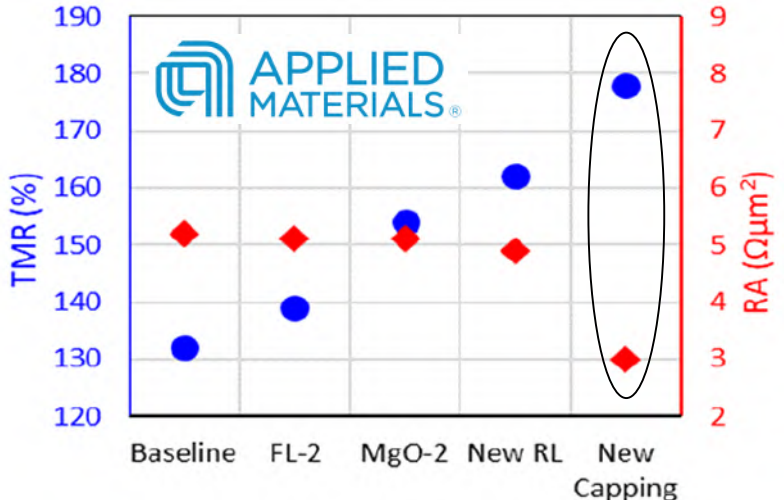
Still used in HDD magnetoresistive reader with RA~0.3Ω.μm² and TMR ~70%

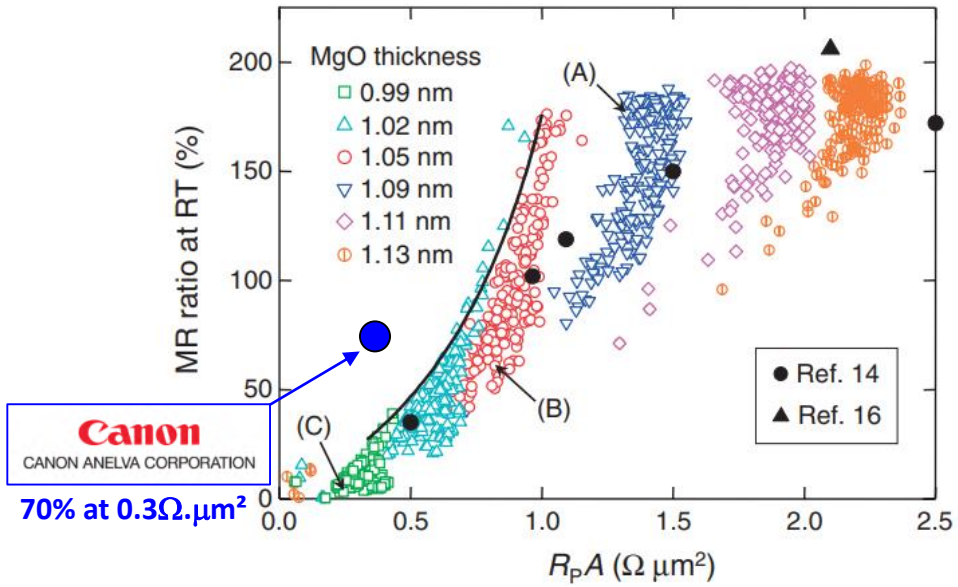
Very low RA MgO-based MTJ

TMR decreases rapidly at low RA (<5Ω.µm²) i.e. at low MgO thickness



S.Yuasa et al, Nat.Mat (2004); doi:10.1038/nmat1257





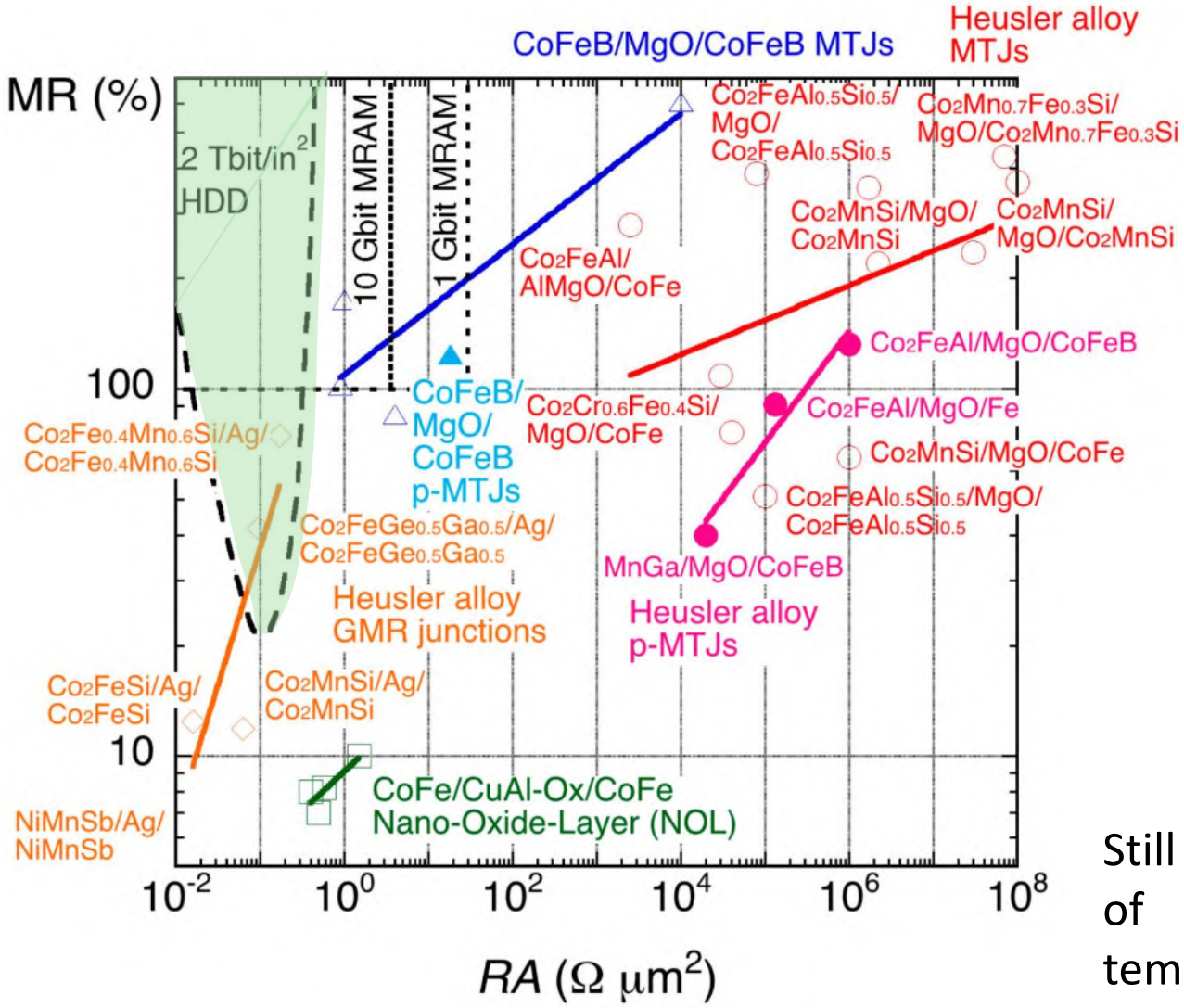
H.Maehara et al, Applied Physics Express 4 (2011) 033002

Range of RA appropriate for STT-MRAM

RF deposited MgO

Range of RA appropriate for TMR heads

For extremely low RA (<0.1Ω.μm²), Heusler alloys based CPP spin-valves



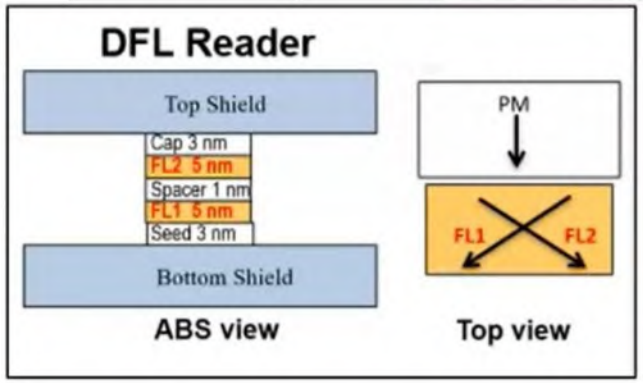
A.Hirohata et al, Materials **2018**, *11*(1), 105;

Still issues with high temperature deposition of Heusler alloys (~400°C while max temperature for MR heads ~250°C) and total thickness of GMR stack.

Advanced Reader Concepts

Design	Stack Type	Cross track dimension (RW < 20 nm)	Downtrack dimension (SSS < 20 nm)	Estimated Signal Level	Main Device Noise Sources	Key Challenges	Device Geometry (side view, ABS view, est SSS)
Bottom Spin Valve (BSV)	TMR	Y	N	> 10 mV	Thermal Mag, Shot, STT	Scaling, SNR, Resistance	24 nm
Bottom Spin Valve (BSV)	CPP-GMR	Y	N	> 1 mV	STT, Thermal Mag, Shot	Scaling, SNR	26 nm
recessed AFM (rAFM)	TMR	Y	Y	> 10 mV	Thermal Mag, Shot, STT	SNR, Scaling, Resistance	18 nm
Dual FreeLayer (DFL)	TMR	Y	Y	> 10 mV	Thermal Mag, Shot, STT	Stability, SNR, Resistance	17 nm
Spin Torque Oscillator (STO)	TMR	Y	N?	> 10 GHz	Phase Noise, Thermal Mag	Scaling, SNR, High Frequency Operation, Stability	24 nm
Non Local Spin Valve (NLSV)	TMR	Y	Y?	> 100 uV	Spin Shot, Thermal Mag	Scaling, SNR, High Impedance Detector, 4-terminal	16 nm

M.Kief
Intermag 2021



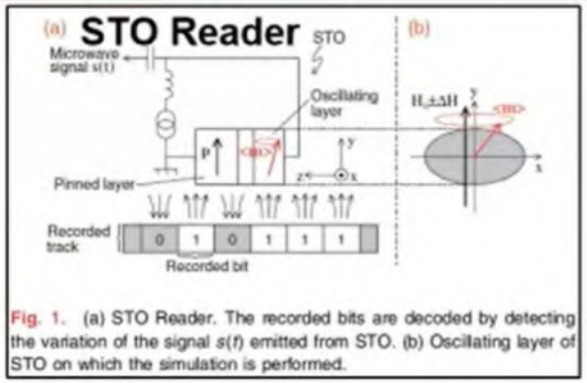


Fig. 1. (a) STO Reader. The recorded bits are decoded by detecting the variation of the signal $s(t)$ emitted from STO. (b) Oscillating layer of STO on which the simulation is performed.

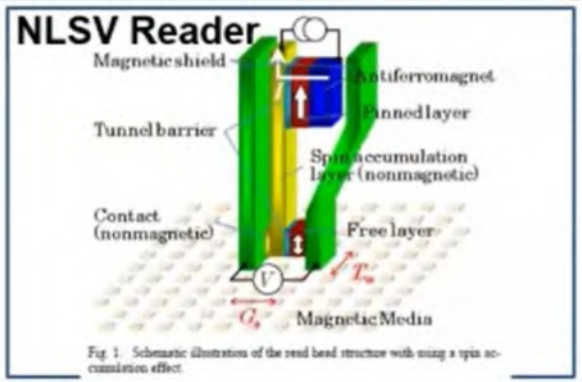


Fig. 1. Schematic illustration of the read head structure with using a spin accumulation effect.

References:

1. Kief et. al,"Dual Freelayer Reader for Improved Linear Density", FE-07, Intermag 2017.
2. Kudo et. al, "Numerical Simulation on Temporal Response of Spin-Torque Oscillator to Magnetic Pulses", Appl. Phys, Exp. 3, 43002 (2010)
3. Yamada et. Al, "Scalability of Spin Accumulation Sensor", IEEE Trans. Magn. 49, 713 (2013).

MR reader roadmap to reach 4TB/inch²

G.Albuquerque et al., "HDD Reader Technology Roadmap to an Areal Density of 4 Tbpsi and Beyond", IEEE trans.Mag.58, 3100410 (2022)

READER ROADMAP TECHNOLOGY CHALLENGES

Reader Challenges	Key Issues	Possible Solutions	Important Research Projects
Signal	MR ~ 100% is required near RA 0.2 ohm.um2 for 2.4 Tbpsi. (assumes 3dB from TDMR) MR >> 100% is required near RA 0.1 ohm.um2 for 4.0 Tbpsi. (assumes 3dB from TDMR)	- Continued optimization of MgO MTJ stack. - Improved/new electrode-barrier/spacer materials and process for increased spin polarization, filtering.	- Understand Low RA/ high MR limits for practical MgO MTJ. - Optimized materials/ process for improved low RA FeCo/MgO stack. - What's after MgO to meet requirements for RA ~ 0.1, high MR? - Improved/new spacer materials for TMR, GMR with oxide/ metal/ semiconductor spacers and high spin polarzation FM (e.g. Heusler) electrodes. - Demo high MR and good uniformity of nano-oxide spacer at 10nm scale.
Noise	Thermal magnetic noise increases rapidly with shrinking Freelayer (FL) volume	- Reduce Freelayer damping constant - Maximize Freelayer saturation magnetization with good anisotropy and low magnetostriction	- engineered Freelayer and cap materials/ interfaces for reduced damping - engineer magnetically soft Freelayer materials near 2.4T
	Shot Noise and Johnson Noise increase for smaller TMR devices.	- Improved tunnel barrier quality for reduced Shot noise, lower RA for reduced Johnson noise (TMR).	- see above
	Preamp noise can be dominant near 1k Ohms	- Low RA, Lower preamp noise.	- develop lower noise preamp for high impedance , high frequency reader (e.g. 1k Ohm, 3 GHz)
SNR	In thermal magnetic noise limit, Spin Valve SNR scales as FL Ms x Utilization / damping	Improved FL materials engineering for high Ms, optimized utilization and low damping.	- engineer Freelayer with very high Ms, low damping and soft magnetics.
		- New device concepts for 4+ Tbpsi with high SNR	- Fundametal modeling and experimental validation scaling behavior and SNR for NLSV, STO and other promising reader concepts. - Demonstrate stable STO operation at 10 nm scale. Develop/ verify high SNR detection method. Scale design for high linear densities. - Model and characterize scaling of signal/ noise in NLSV to 10nm scale with <10nm thick channel. Develop very high impedance, high freq detector preamp. Evaluate feasability of Graphene based NLSV.
Downtrack Resolution	Reader Gap (RG) or shield to shield spacing needs to scale with linear density. BSV RG is near 25nm. rAFM RG may approach ~ 18nm. Reduced RG < 15nm is needed >~3500kBPI.	- Reduce reader stack thickness at ABS. (Thinner FL, SAF, AFM, seed, cap layers) - Enable/ improve recessed AFM SV design	- Thinner AFM, SAF, cap/ seedlayer with equal or better properties. - Controlled SAF stiffness in rAFM.
		- New device concepts with reduced RG	- Experiments and modeling to evaluate STO, NLSV and other promising reader concepts for shield to shield spacings at < 15nm. - Invent and develop new high resolution concepts for linear densties > 3500 kFCI
	HMS is not scaling with AD which drives RG lower to meet P50 requirements.	- Enable lower reader magnetic spacing.	
Crosstrack Resolution	Reader width must decrease < 10nm for >~1100 kTPI	- Improved formation processes for lower sidewall damage	- characterization and correlation of edge damage/ defects with degraded MR and micromagnetics. - improved low damage etch for <10nm devices.
	MT10/MT50 increases with decreasing RW.	- Improved side shield materials, thin gap.	- higher permeability side shield materials
	HMS is not scaling with AD which drives RW lower to meet MT10 requirements.	- Enable lower reader magnetic spacing.	
Stability/ Reliablity	Spin torque instabilites can limit reader current density and signal.	- Mitigate instabilities with reduce spin torque and/or increased damping in FL	- materials and stacks to reduce STT in GMR sensors
	Freelayer materials with high Ms and/or high spin polarization often have high magnetostriction.	- New/improved lower magnetostriction materials with high Ms, high polarization (e.g. Heusler)	- engineer materals film, multilayers and/or interfaces for low effective magnetostriction
		- Control reader stress.	- How to engineer device stress?
Manufactur-ability	Need high yields for growing complex device with CD < 10nm	- Improved formation processes.	- lower damage etch with reduced power and/or RIE while maintaining junction profile and CD sigma.
	High resistance range for nano-oxide based spacer devices.	- Spacer with homogeneous spin conduction.	- Develop nano-oxide spacer (or similar) with low variance at nm scale.
	Multiple readers add process content and cost	- Novel concepts to reduce process content	- Narrow pitch etch process.

IDEMA consortium

Magnetic media

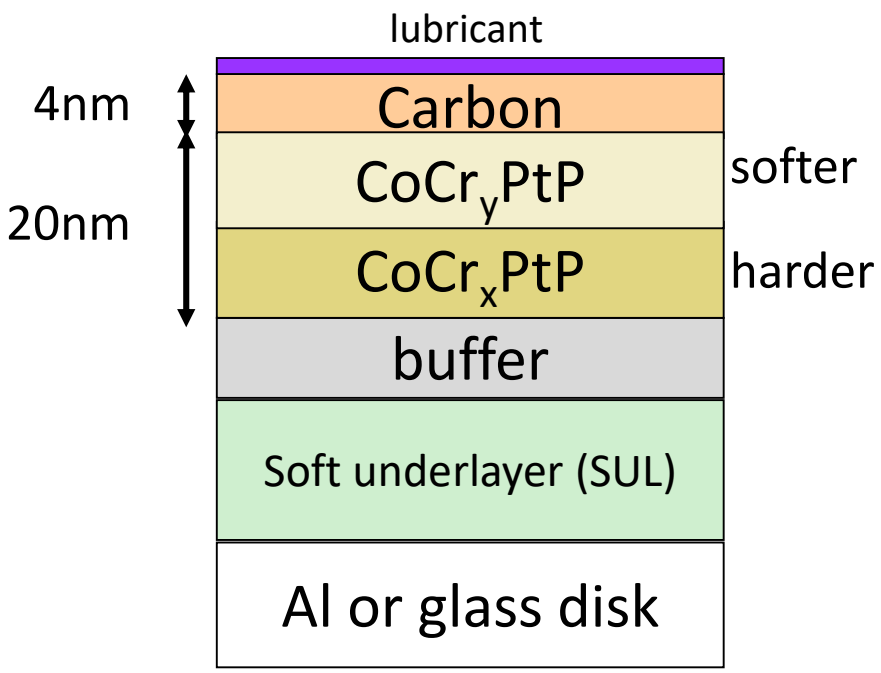
Required properties :

- Granular media, grain size ~5nm, decoupled grains
- High M_{sat} , Square hysteresis loops (M_r/M_{sat}>0.9)
- Large H_c (>0.4T)
- Longitudinal media until 2004, perpendicular media (PMA) since 2004

⟶ CoCrPtX

Exchange coupled composite media (ECC media) :

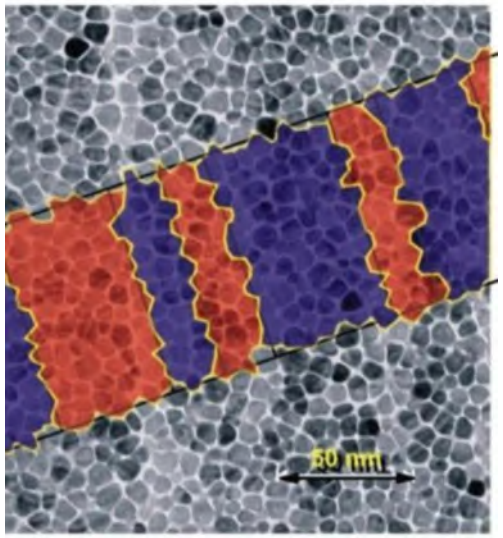
The magnetization reversal is nucleated in the softer layer and then propagates in the harder layer



R.Victora, IEEE Trans.Mag. 41, 537 (2005)

hcp, c-axis out-of-plane

Pt: Higher anisotropy (strong spin-orbit coupling)
Cr, P : Diffuse towards grain boundaries and decouple the grains.

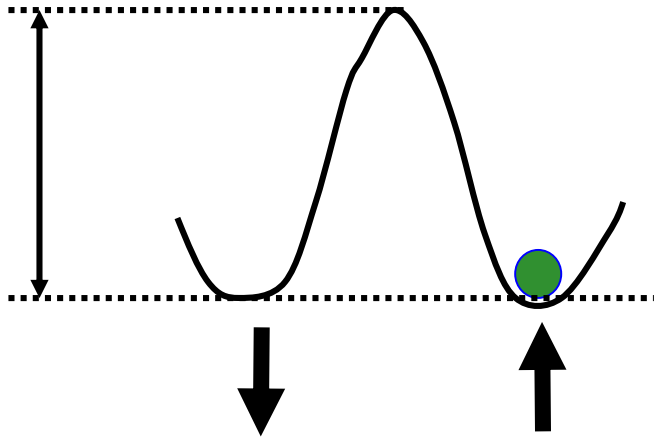


- **Roughness of bit transitions determined by grain size.**

-> **Need to decrease grain size to increase areal density.**

Superparamagnetic limit in recording media

Two possible states for the magnetization of each grain

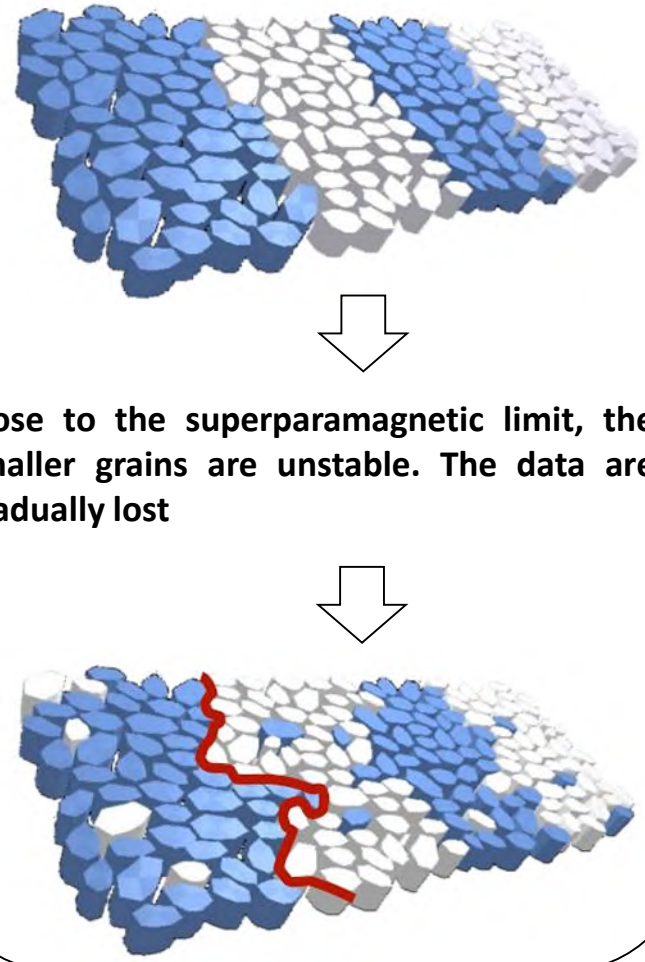


Barrier due to uniaxial anisotropy: $\Delta E = K_u V$

$$\tau = \tau_0 \exp\left(\frac{\Delta E}{k_B T}\right)$$

Characteristic flipping time

Attempt time ~10^{-9} sec.



Close to the superparamagnetic limit, the smaller grains are unstable. The data are gradually lost

Stability of the stored information over 10 years at 80°C implies

$$\left(\frac{K_u V}{k_B T}\right) > Ln\left(\frac{10\,years}{10^{-9}\,\mathrm{sec}}\right) \quad \text{i.e.} \quad \boxed{K_u V > 40 k_B T}$$

Superparamagnetic limit in recording media (cont'd)

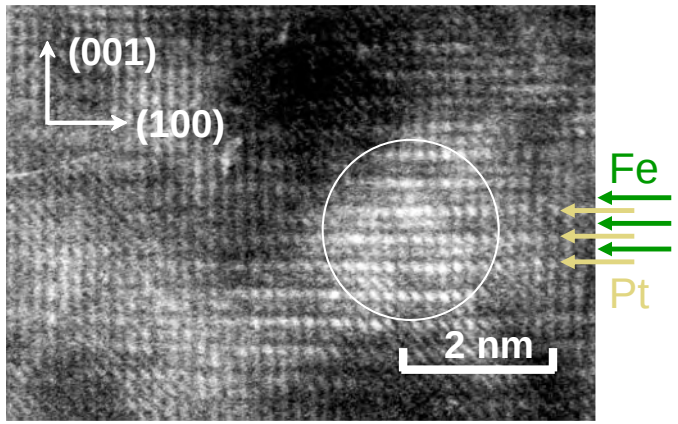
Decreasing grain size : ⇒ Need to increase anisotropy to maintain $K_{uniaxial\ anisotropy}$*grain volume > 40 k_BT

In CoCrPt, $K_{uniaxial\ anisotropy}$~ $4.10^5 J/m^3$. Minimum grain size ~7nm

At 1Tbit/in², bit length~15nm i.e. ~ **2 grains in a bit length** ! 6 grains crosstrack

Hard to further decrease the grain size and bit length with conventional CoCrPtX media !!!

There exist magnetic material with larger perpendicular anisotropy e.g. L10 ordered FePt alloys



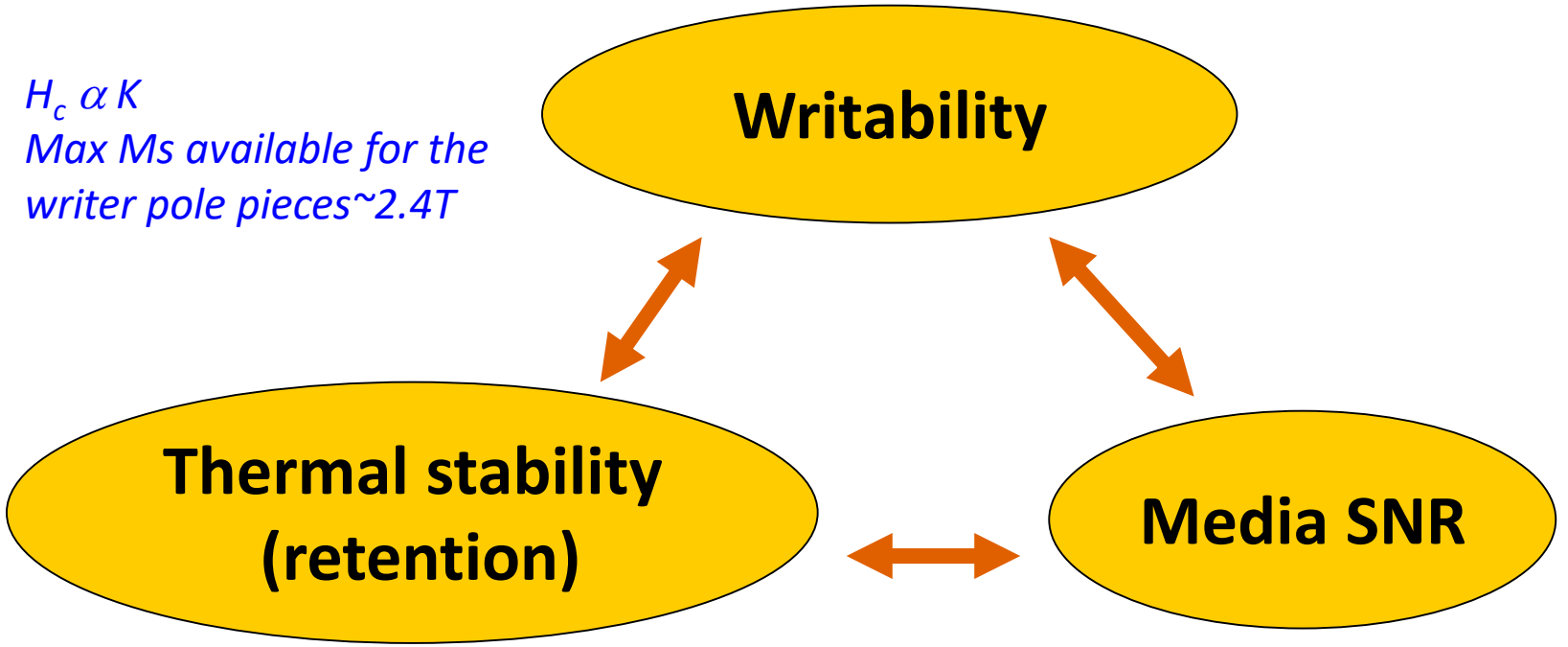
Grains magnetically stable down to 3nm

<u>But :</u> Anisotropy ↗ ⇒ field required to write ↗ (~2.5T for FePt)

However, maximum field produced by write head determined by magnetization of pole piece ~ 1.5T for the best known materials (FeTaN)

⇒ Impossible to write in FePt at 300K.

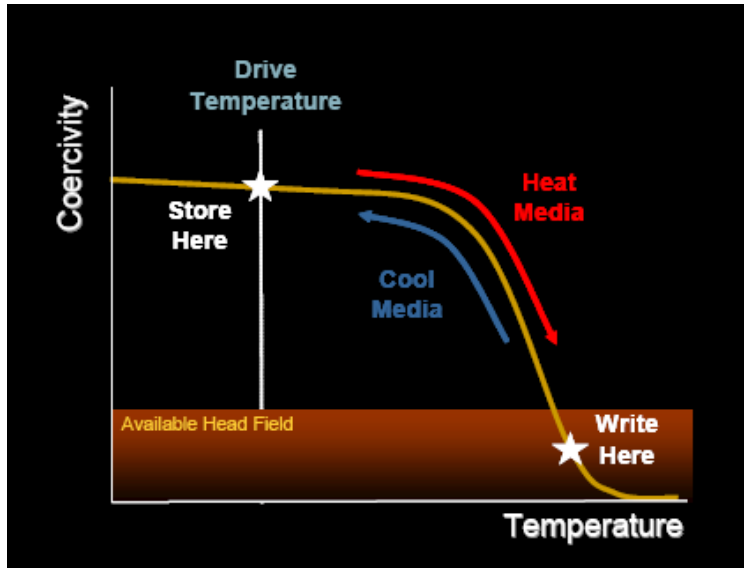
Magnetic recording trilemma



How to get around this trilemma and keep on increasing the areal density ?

- Energy assisted recording (by microwave (MAMR), by heat (HAMR))
- Patterned media

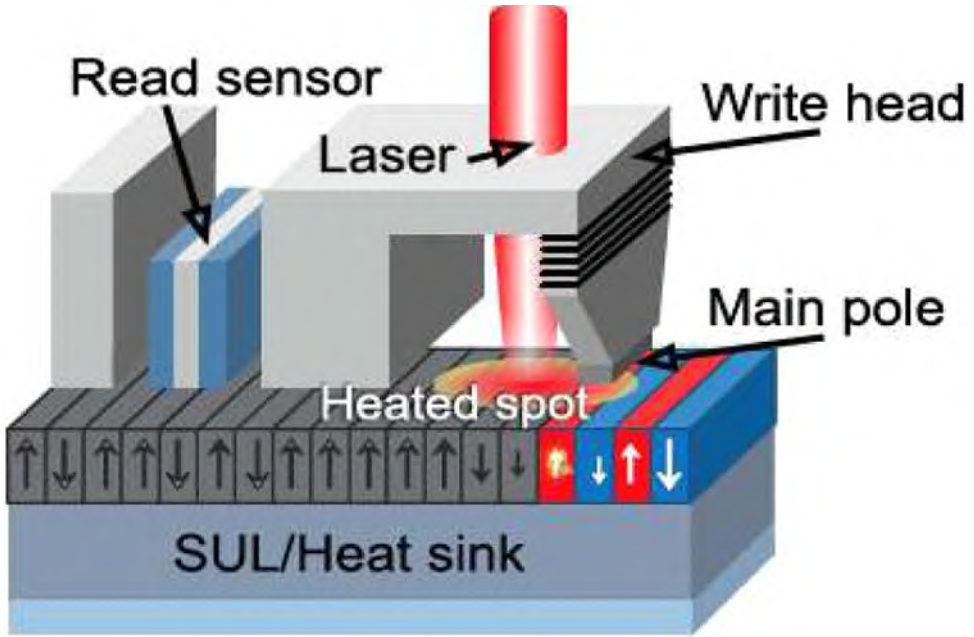
1st approach : Heat Assisted Magnetic Recording (HAMR)



From Seagate

Combination of heating and application of magnetic field.

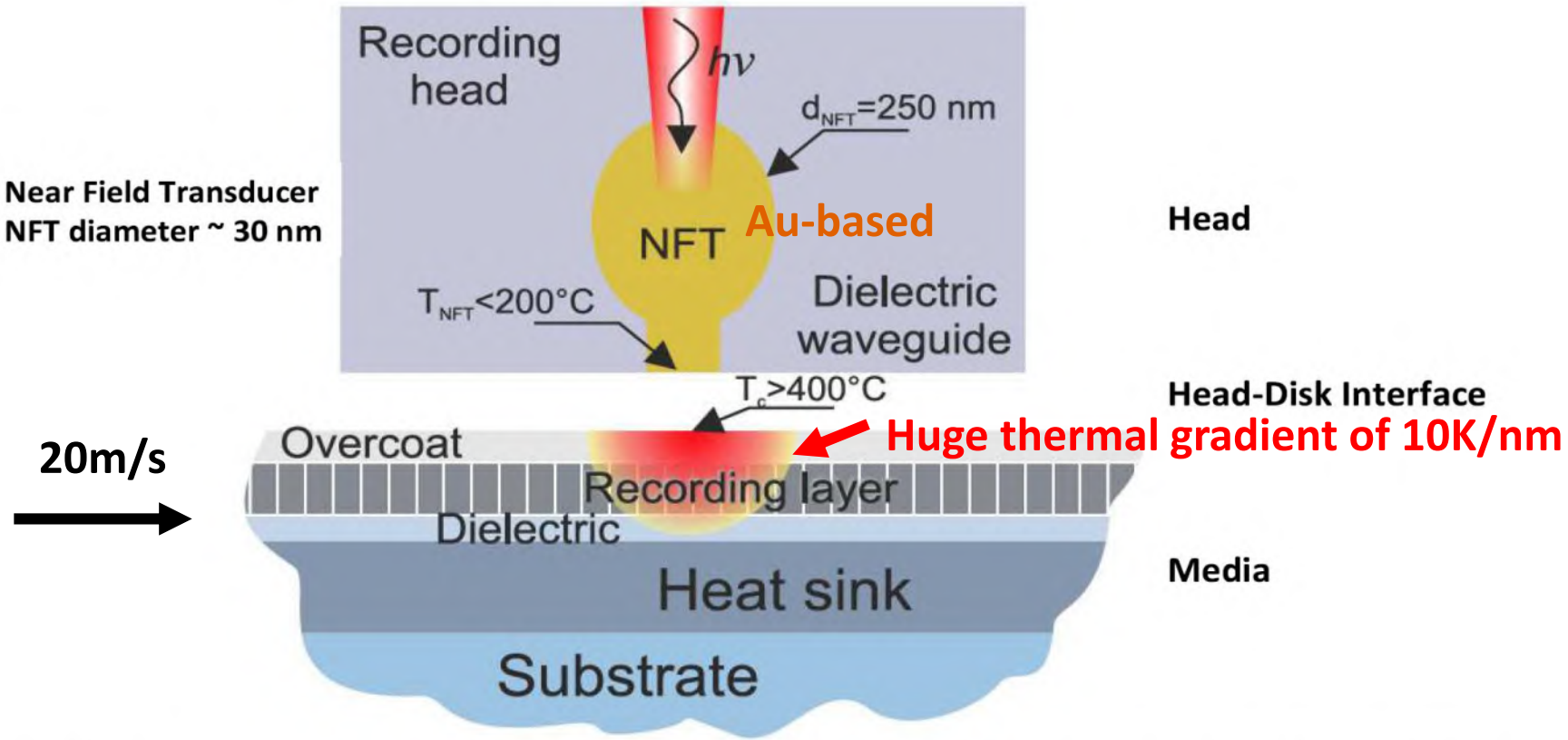
Write at high T with reduced anisotropy
Store at RT with high anisotropy



Difficulty: heating of a region of ~20nm with strong thermal gradient.

Heat provided by **laser and near-field plasmonic antenna**

HAMR / Local heating produced by plasmonic antenna



W.A.Challener et al, Nature Photonics 3, 220 (2009)
D.Weller et al, J.Vac.Sci.Technol. B 34, 060801 (2016)

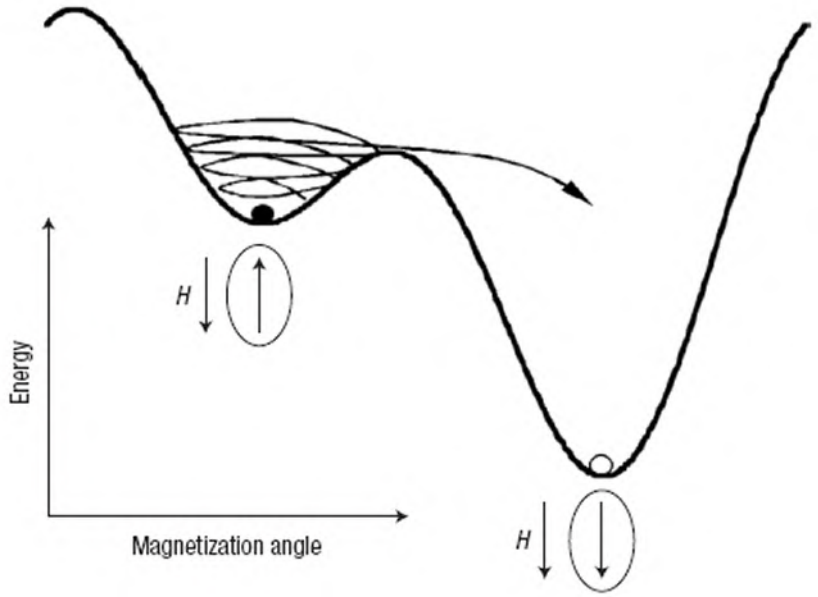
Media heated just above T_{curie} Magnetization builds up in the applied field upon cooling below Tc

A key difficulty in HAMR is the reliability of the plasmonic transducer
Commercial products announced by Seagate

2nd approach : Microwave Assisted Magnetic Recording (MAMR)

Basic idea: assist field induced switching by a microwave excitation of the magnetization

Thirion, C., Wernsdorfer, W. & Mailly, D. Nature Mater 2, 524–527 (2003).



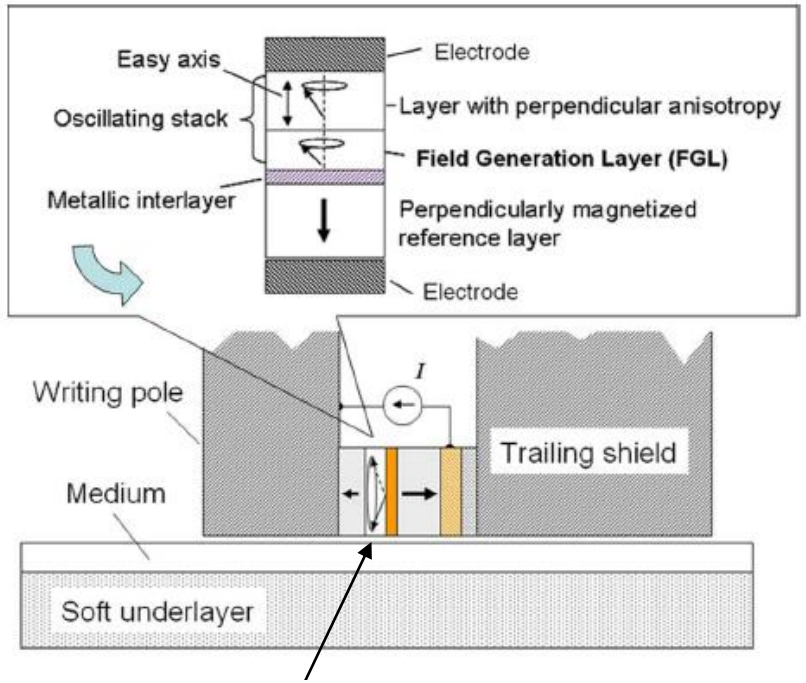
- Magnetization precesses under the effect of the microwave.
- If the microwave frequency is close to the ferromagnetic resonance frequency, the magnetization absorbs the microwave energy faster than it dissipates it.

- →Increase in energy which allows the magnetization to climb anisotropy energy barrier and switch despite $H<H_K$.

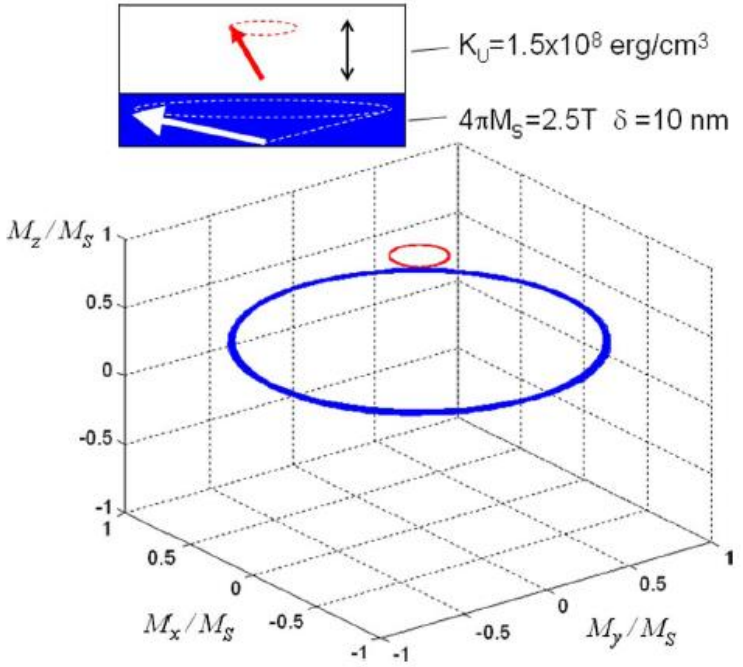
Important role of excitation frequency (~30GHz) and of Gilbert damping in media

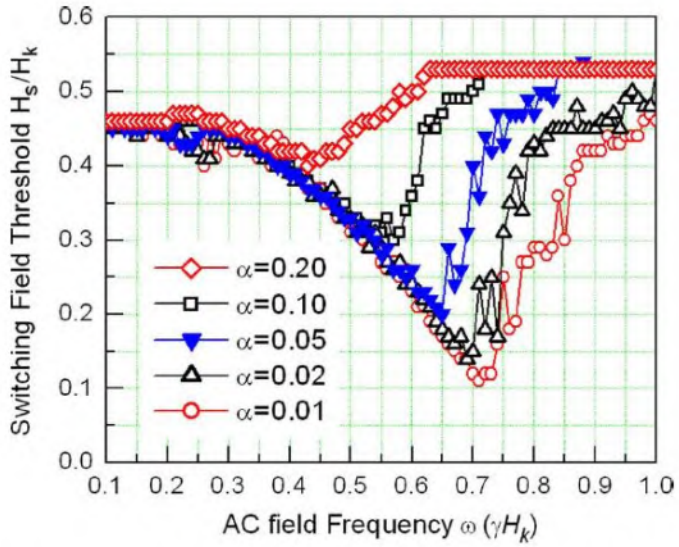
2nd approach : Microwave Assisted Magnetic Recording (MAMR)

- Spin transfer oscillator inserted in the write gap of the write head
- DC Current flowing between main pole and trailing shield



RF field generated by the precession of the STO free layer magnetization





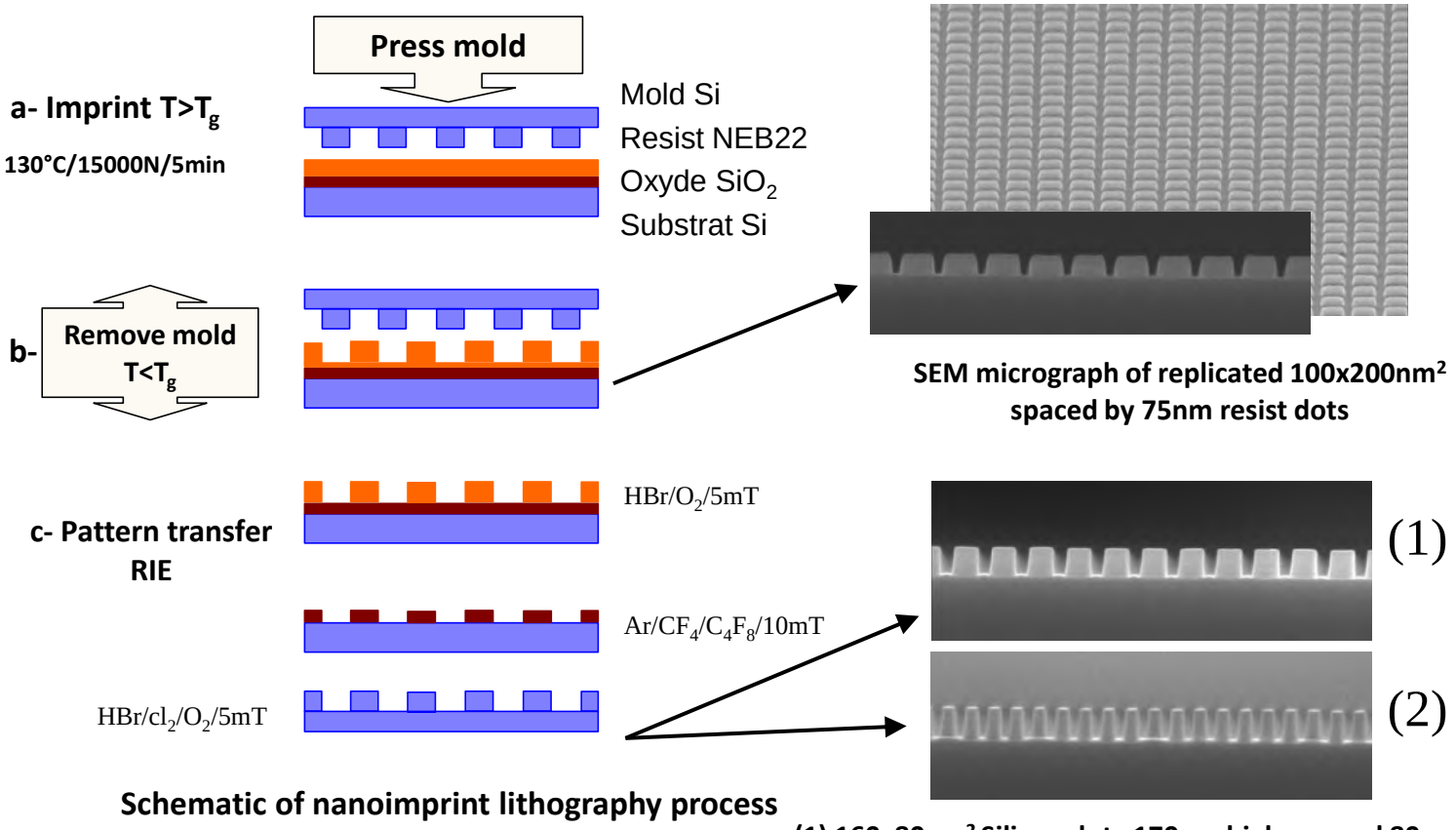
Calculated switching field threshold as a function of ac field frequency for a series of damping constant values. The pulsed reversing field is at 30° angle w.r.t. easy axis and the ac field amplitude is 0.1 H_k.

(J.Zhu IEEE Trans Mag 2008)

Commercial products developped by Western Digital

Patterned media : media nanostructured at the bit scale

Media nanostructured in an array of dots. 1 dot =1 grain= 1bit

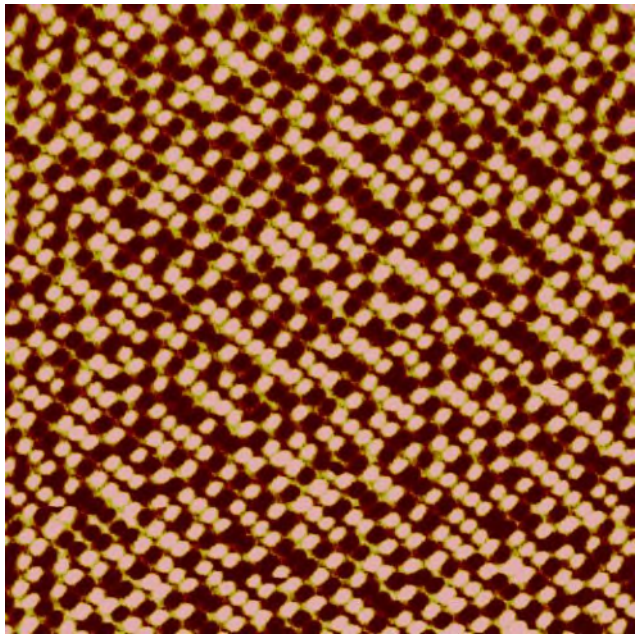


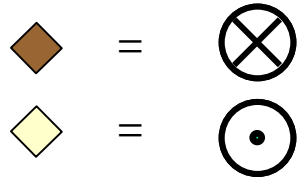
SEM micrograph of replicated 100x200nm² spaced by 75nm resist dots

Schematic of nanoimprint lithography process

(1) 160x80nm² Silicon dots,170nm high, spaced 80nm

(2) 80x80nm² Silicon dots,170nm high, spaced 65nm

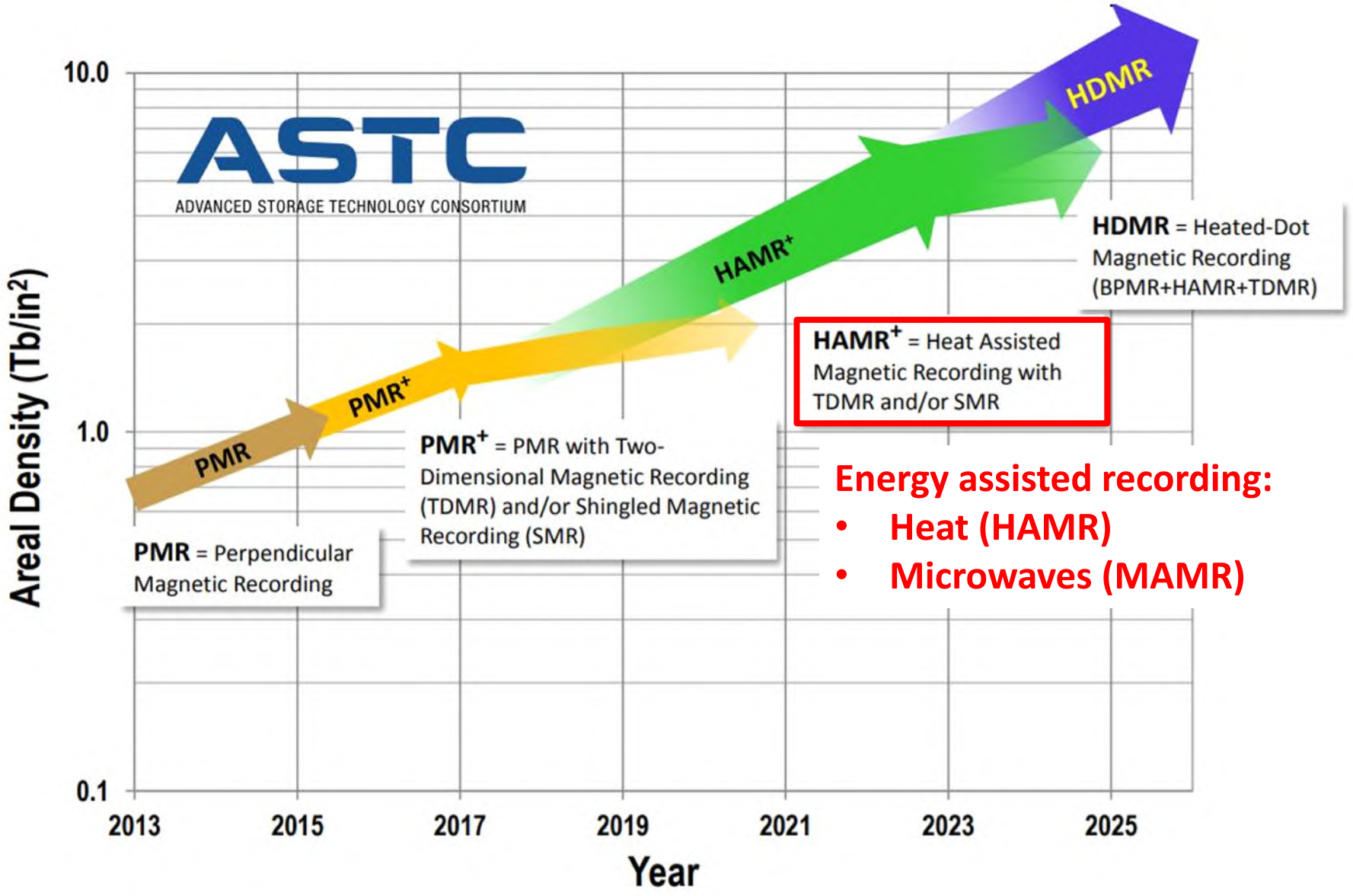




Patterned media technology was proven to work well in the lab….
but not economically viable (too costly/competing technology)

B.Terris et al, J. Phys. D: Appl. Phys. **38** (2005) R199–R222

Magnetic recording roadmap

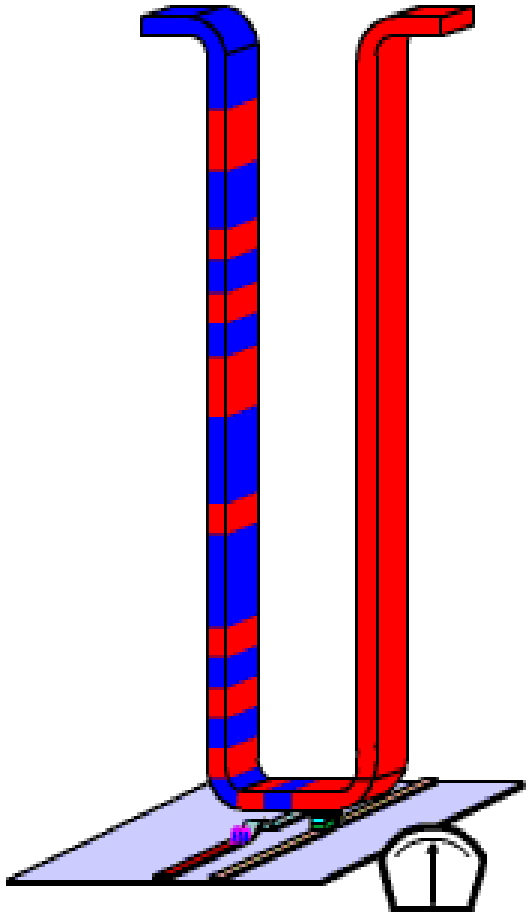


Energy assisted recording:

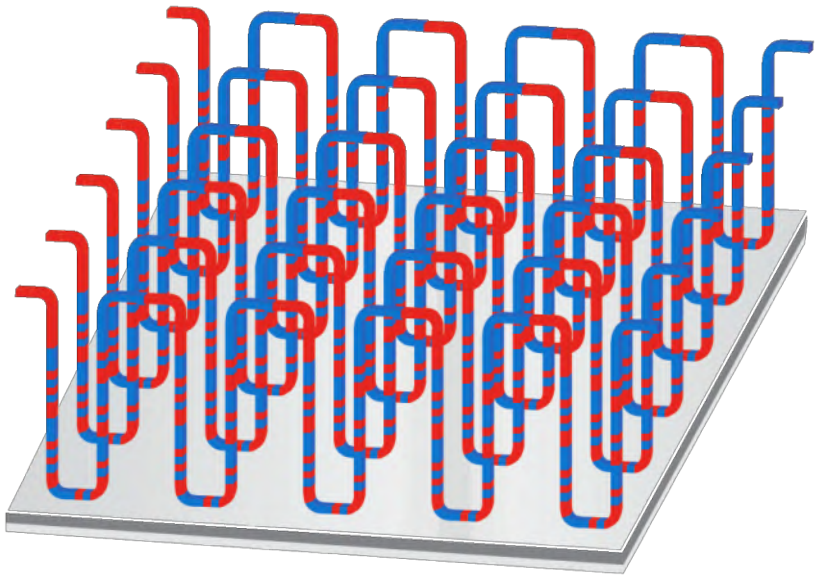
- **Heat (HAMR)**
- **Microwaves (MAMR)**

Magnetic racetracks based on domain walls or skyrmions

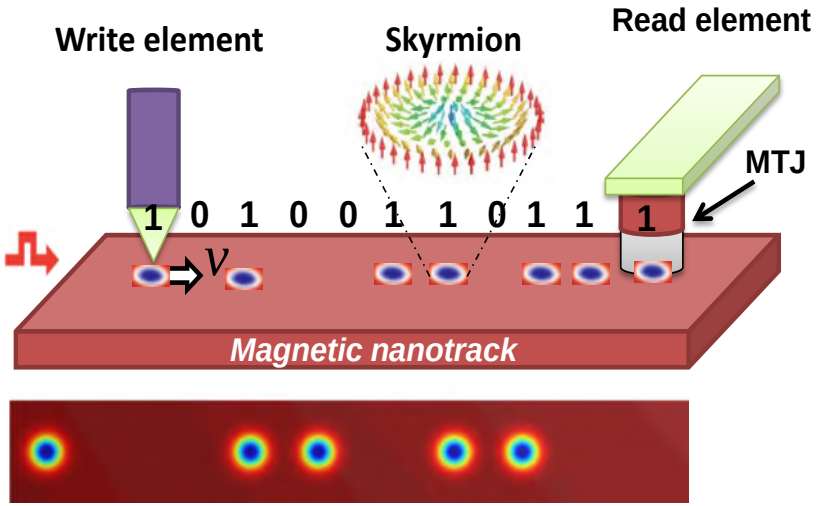
A shift register memory based on current induced propagation of magnetic textures.
Advantages over HDD: No moving parts (i.e. robustness) and possibility to go 3D



S. S. P. Parkin, Science 320, 190 (2008) + patents (IBM)

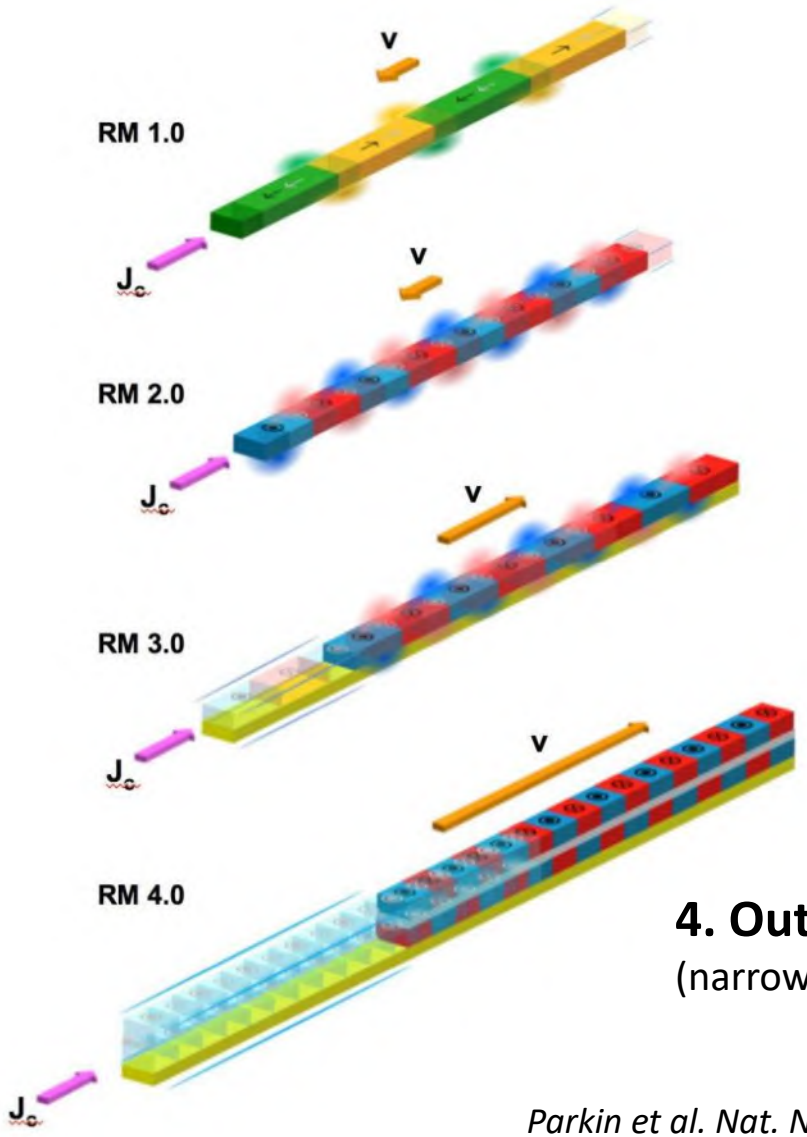


Dreaming of a 3D storage device



*Romming et al., Science **341**,636 (2013)*
Fert, A et al, Nat. Nanotech. 8, 152 (2013)
Sampaio et al, Nat. Nanotech. 8, 839–844 (2013)

Significant progresses made since 2008…



1. In-plane magnetized racetrack

(large domains, wide DW, DW slow (~few tens m/s) and changing configuration)

2. Out-of-plane magnetized racetrack, DW moved by bulk STT

(narrower DW, faster DW (100m/s), high current density required for propagation)

3. Out-of-plane magnetized chiral racetrack with DMI, DW moved by SOT

(narrower DW, faster DW (300m/s), moderate current density required for propagation)

4. Out-of-plane magnetized chiral SyAF racetrack with DMI, DW moved by SOT

(narrower DW, faster DW (1000m/s), moderate current density required for propagation)

Parkin et al. Nat. Nanotechnol. 10, 195-198 (2015)

Conclusion on magnetic recording

- At present areal density ~1Tbit/in², bit size ~15nmx40nm.

- Reader now based on low resistance MgO tunnel junctions (RA~0.3Ωμm²) with tunnel magnetoresistance ~ 70%. CPP-GMR with Heusler alloys based MTJ will likely be used below RA~0.1Ωμm²

- Energy assisted technologies developed to overcome the trilemma limit of recording : MAMR, HAMR.

- Increasing competition with Flash SDD but HDD still ahead in terms of cost/Gbit. Tape recording is benefiting from all progresses on HDD technology. These 3 technologies complement each other and will keep on coexisting (portable application for SDD versus static application with large capacity for HDD).

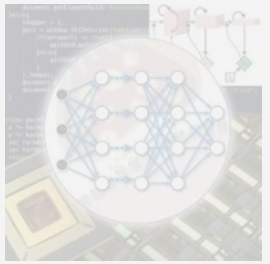
- Racetrack is a challenging technology from the point of view of reliability and « killer application » unclear. Importance of benchmarking with 3D-Flash technology.

Spin-electronics can help !

- Data storage thanks to steadily increasing areal density on hard disk drives

- **Non-volatile magnetic memories (MRAM) to reduce power consumption and speed up communication between logic and memory**

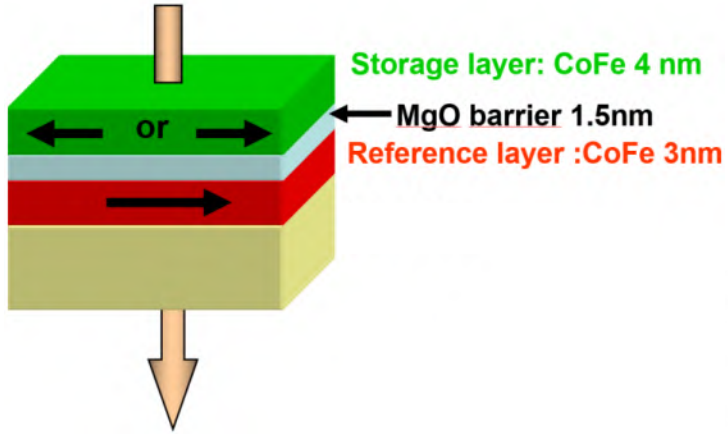
- Neuromorphic architecture to improve computing efficiency for specific applications

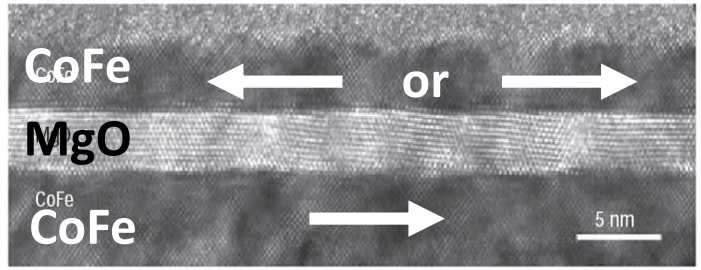


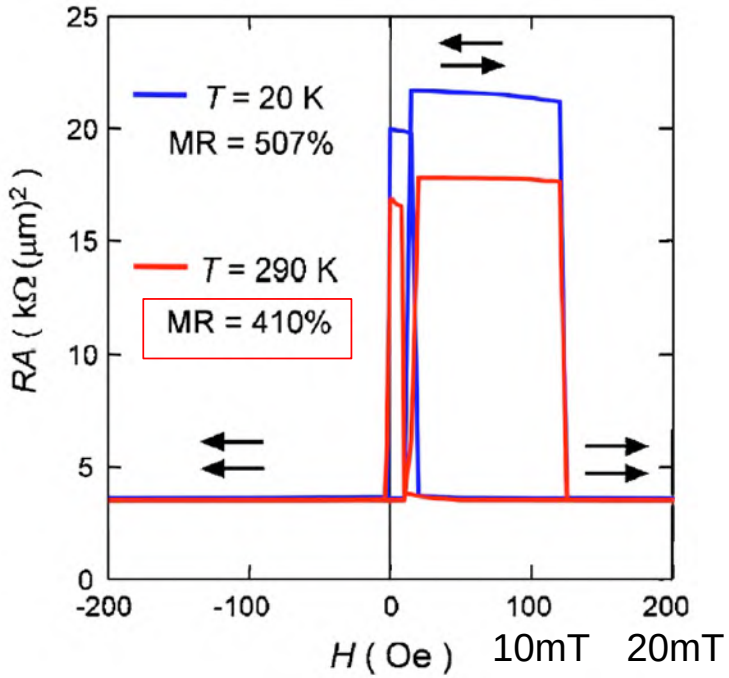
Magnetoresistance of magnetic tunnel junctions (TMR)

Moodera et al, PRL (1995);
Myazaki et al, JMMM(1995).
S.S.P.Parkin et al, Nature Mat. (2004), nmat1256
S.Yuasa et al, Nature Mat. (2004), nmat 1257

MgO-based crystalline junctions







Advantages of TMR compared to GMR for microelectronics:

- **Larger amplitude of the resistance variation** (up to 600% at 300K)
- **Larger resistance than with metallic multilayers** (a few KΩ vs a few Ω) allowing to connect in series silicon transistors (FET) and magnetic tunnel junctions.

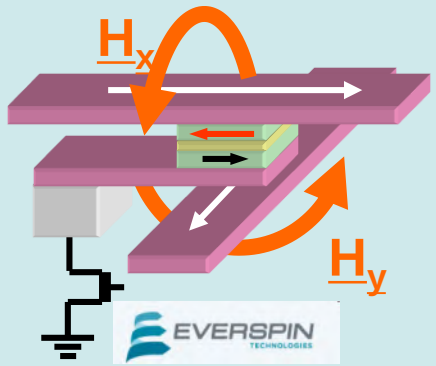
Yuasa et al, APL89, 042505(2006)

The TMR phenomenon allows reading out the magnetic state of magnetic tunnel junctions from their resistance value

« 0 » ↔ parallel configuration ↔ low resistance **« 1 » ↔ antiparallel configuration ↔ high resistance**

The 2nd big industrial application of spintronics : MRAM

Field-driven MRAM

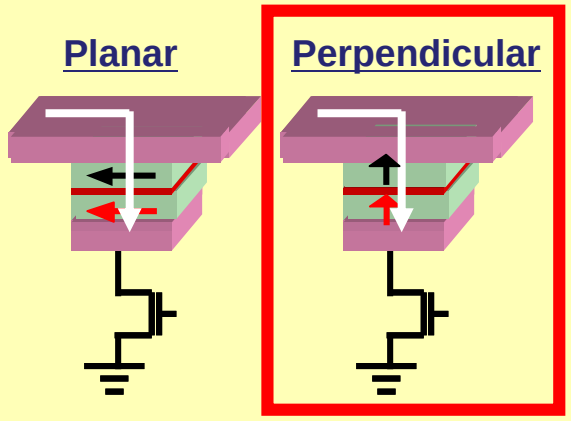


Toggle MRAM

Cell size=1.55 μm^2=(1.24 μm)²
(4Mbit EVERSPIN, GE05, Intermag2004)

Commercialized since 2006 (1Mb, 2Mb, 4Mb, 8Mb, 16Mb) but not scalable. Large power consumption due to field writing.

STT (STT MRAM)

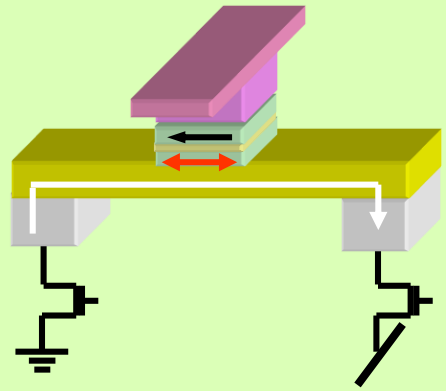


Cell size=0.0084 μm^2=(91nm)²
(demo IMEC, TMRC2020)
Cell size=0.036 μm^2=(189nm)²
(Production 1 Gbit Samsung, IEDM2019)

Commercialized since 2012. Now in production @ all major microelectronics foundries

Spin-orbit torque

(spin-Hall, Rashba)

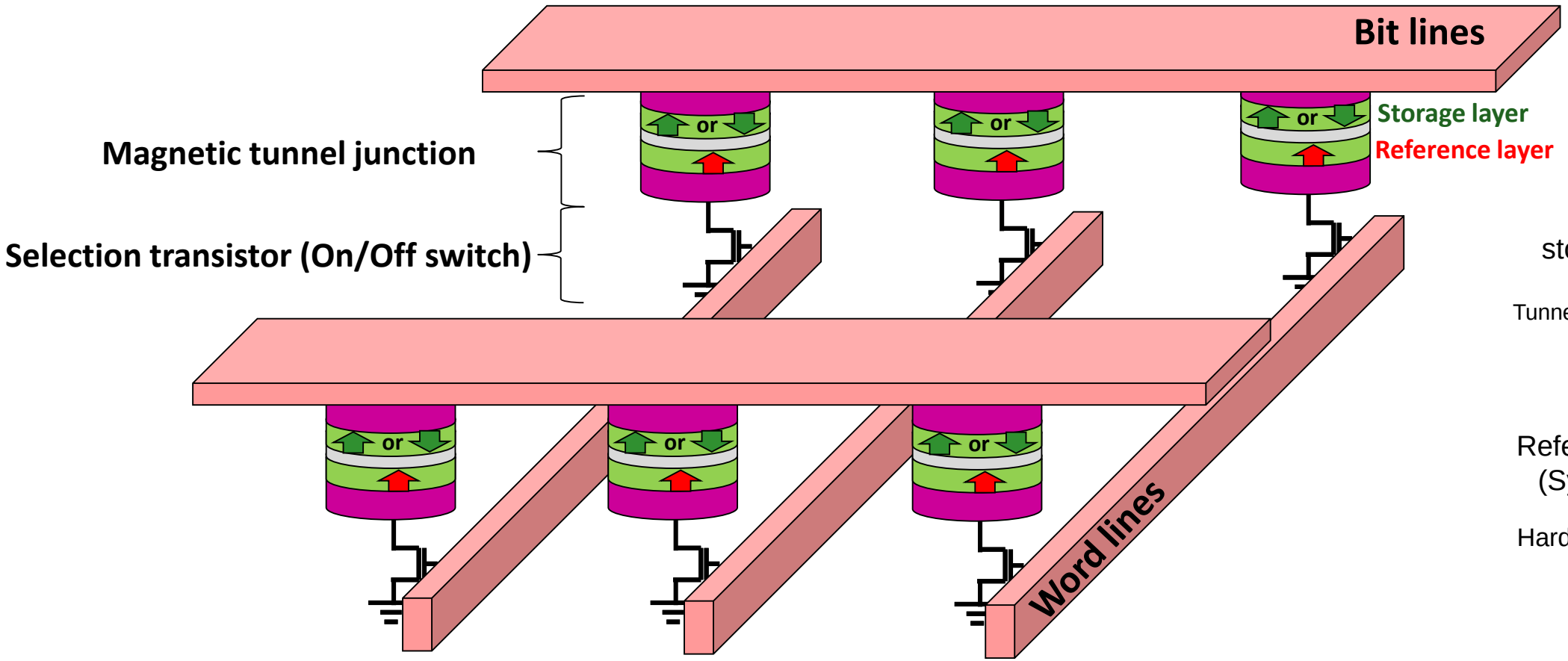


Cell size = 0.021 μm^2=(145nm)²
(demo IMEC, TMRC2020)

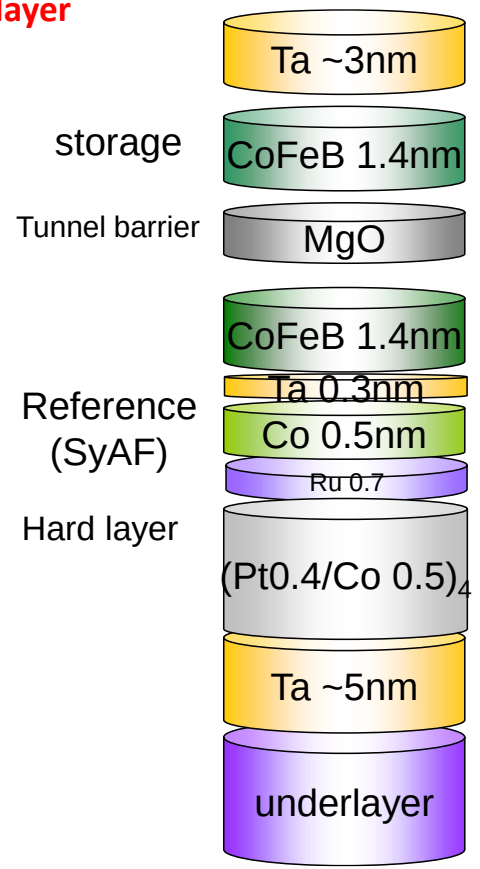
Still under R&D for fast, very endurant memory application.

The out-of-plane magnetized MTJs offer better downsize scalability of STT-MRAM and better tradeoff between retention and writability than for in-plane magnetized MTJs

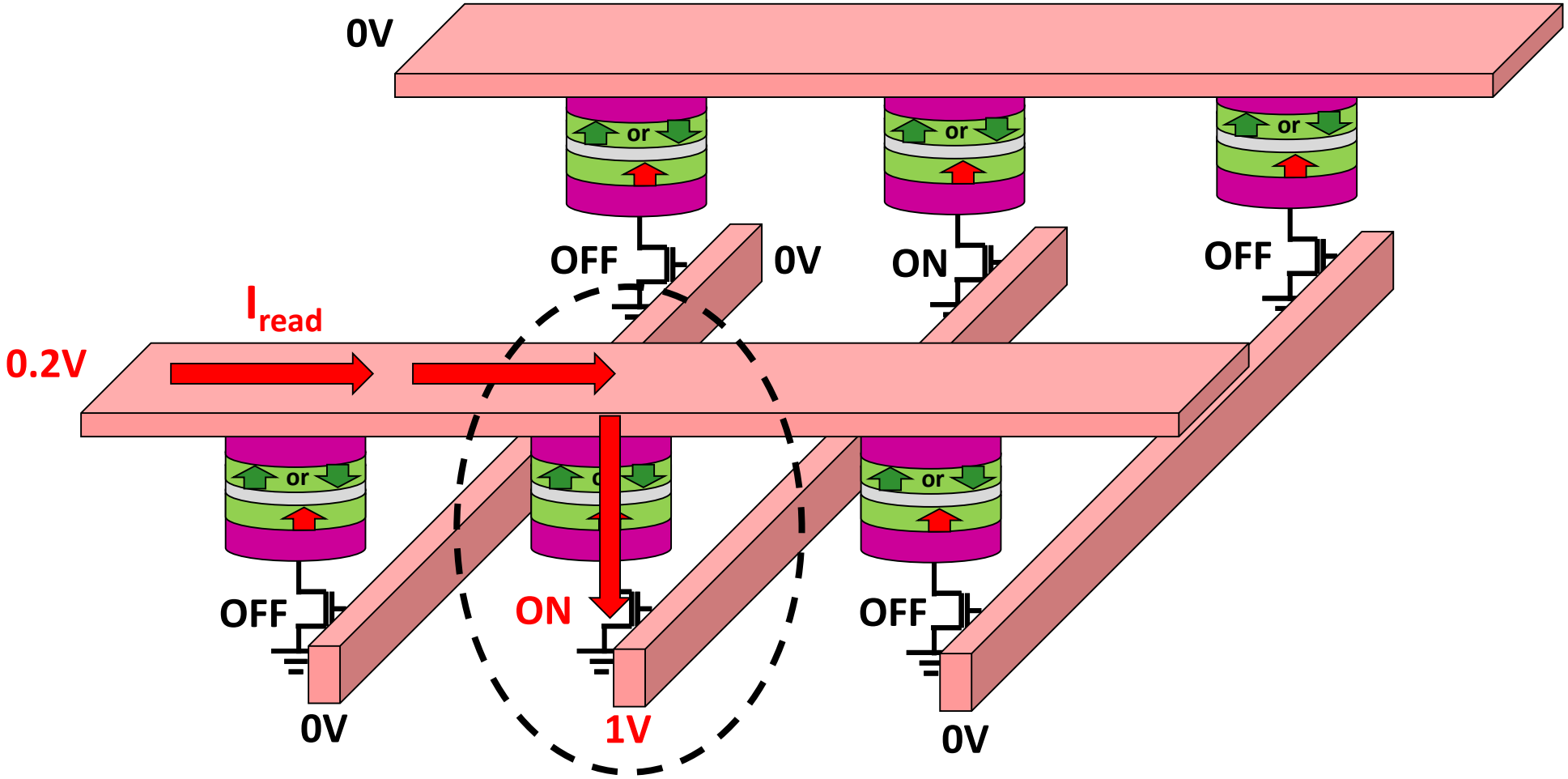
Memory array based on magnetic tunnel junctions



Detailed composition of a magnetic tunnel junction



Reading :

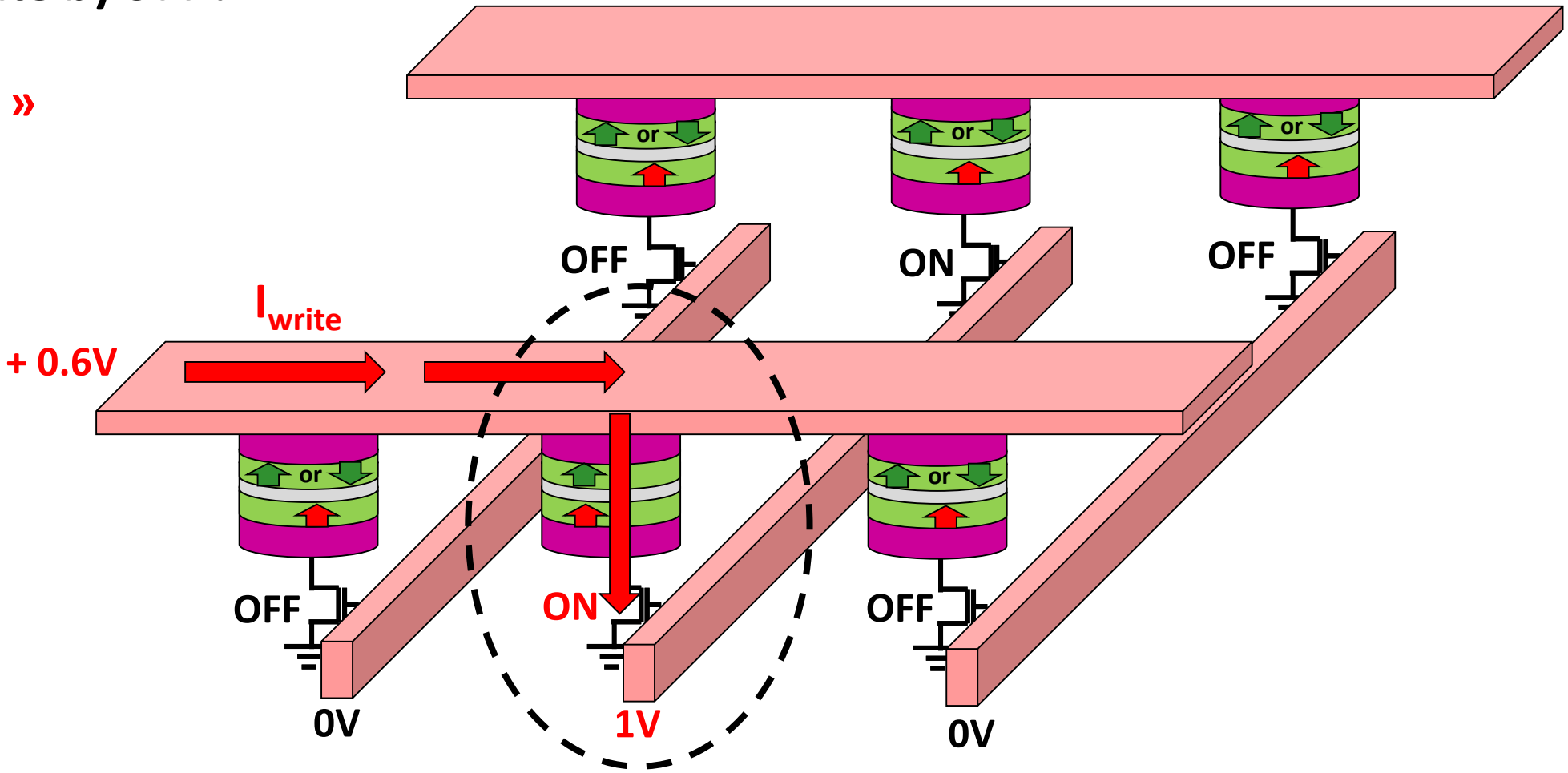


How to write ?

Memory array based on magnetic tunnel junctions

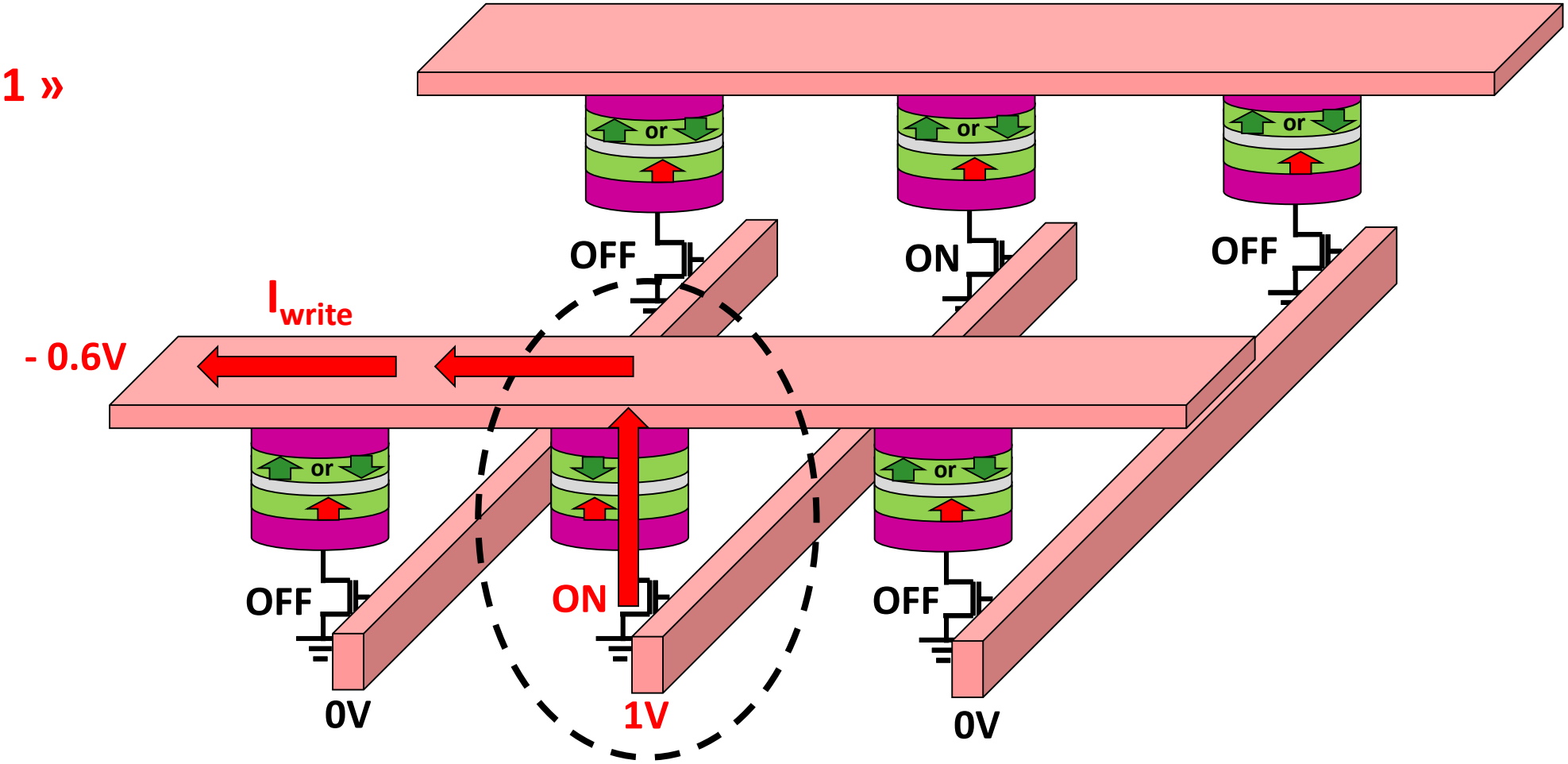
Write by STT :

« 0 »



Write by STT :

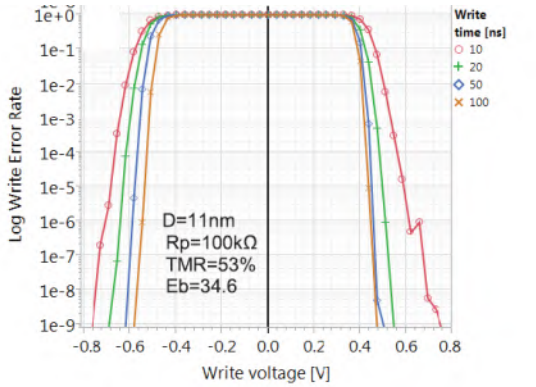
« 1 »

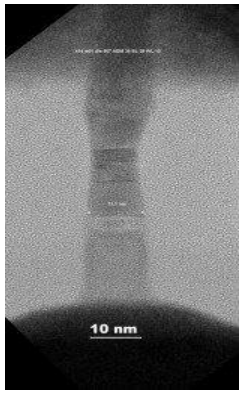


Spin transfer torque magnetic random access memory

STT-MRAM assets :

- **Non-volatility**
- **sub-20nm scalability**
- **Write speed**
- **Write endurance**

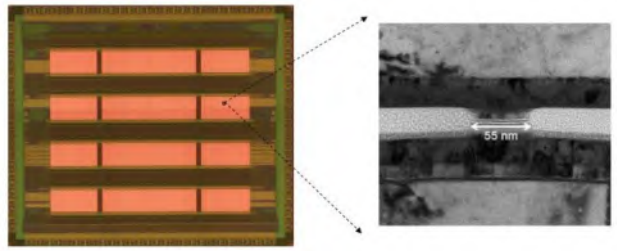


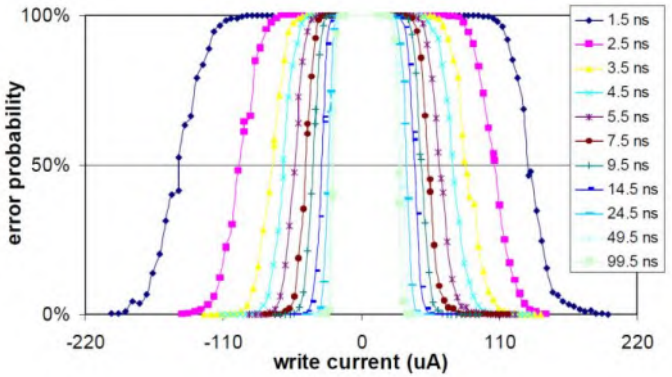


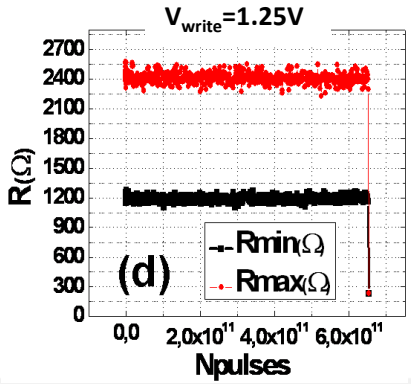
11nm STT-MRAM cell (IBM)
Janusz et al, IEEE Mag.Lett.7, 3102604(2016)

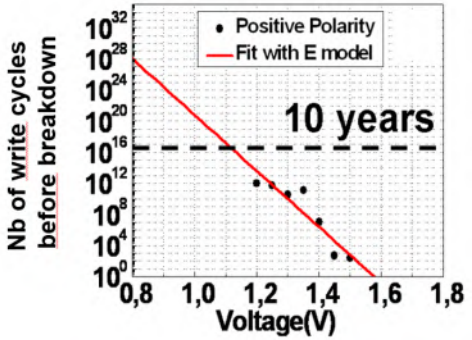
5nm STT-MRAM cell (SPINTEC)
N.Perrissin et al, Nanoscale.10, 12187 (2018)

8 Mbit fully functional demo from TDK/Headway Techno now transfered to TSMC









Quasi unlimited endurance at normal operating voltage ~ 0.6V

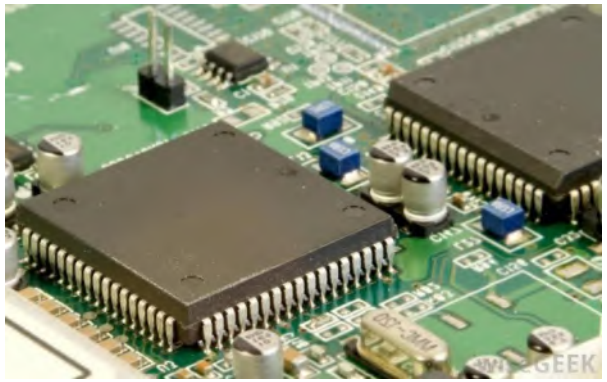
An increasing number of industrial actors active in the MRAM arena

STT-MRAM first application : Embedded Flash replacement

Advantages :

Fabrication of STT-MRAM requires 3 levels of masks instead of 15-20 masks for eFLASH + much better endurance (>10^{12} vs 10^{5}) + much faster write (40ns vs 100µs)+ much reduced energy (400x reduction)

eNVM is a must for **Microcontrollers (µC)** products .
Market segments: Automotive (>50%); Smart Cards; Consumer Applications



- **1Gbit High Density Embedded STT-MRAM in 28nm FDSOI Technology** ,

K. Lee et al , Samsung Electronics Co
Endurance >10^{10} cycles (versus 10^{6} in 2018) , 10 years retention

- **Manufacturable 22nm FD-SOI Embedded MRAM Technology for Industrial-grade MCU and IOT Applications**

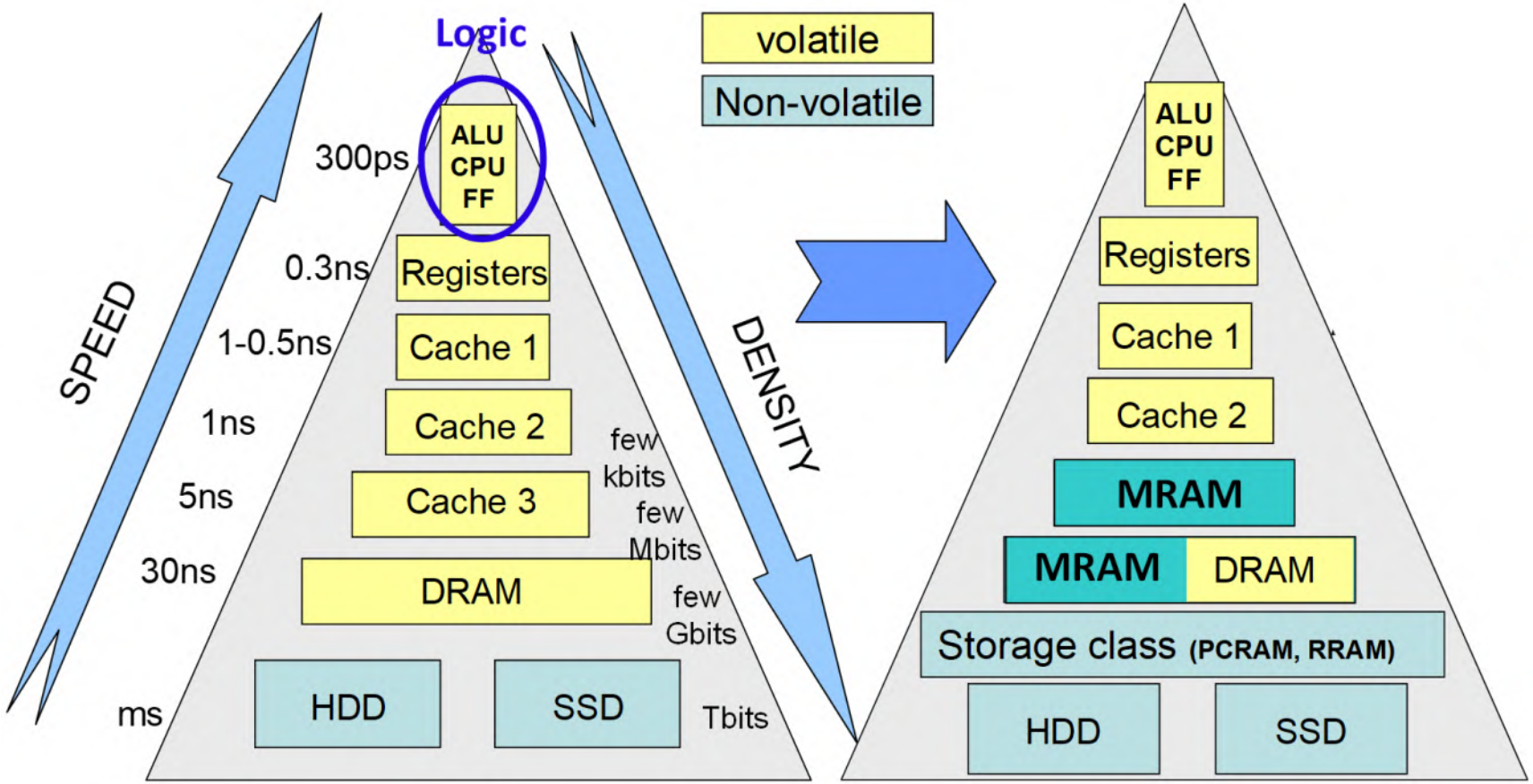
V.B.Naik et al, GLOBALFOUNDRIES
-40~125 °C operating range. 10^{6} endurance and 5x-solder reflows

IEDM 2019

- **22nm STT-MRAM for Reflow and Automotive Uses with High Yield, Reliability, and Magnetic Immunity and with Performance and Shielding Options**

W.Gallagher et al, TSMC
-40 to 150°C operation, ten-year native magnetic field immunity >1100 Oe at 25°C at 1ppm bit upset level

MRAM in the memory hierarchy to reduce static power consumption



Replace part of the volatile working memory (part of DRAM, Last level Cache SRAM) by a non-volatile memory (MRAM).

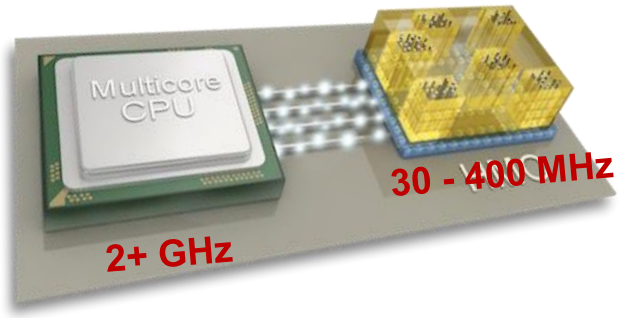
Allows to switch off all temporarily unused blocks of electronic circuits (e.g.microprocessors) thus reducing leakage

→ Normally-Off/Instant-On electronics

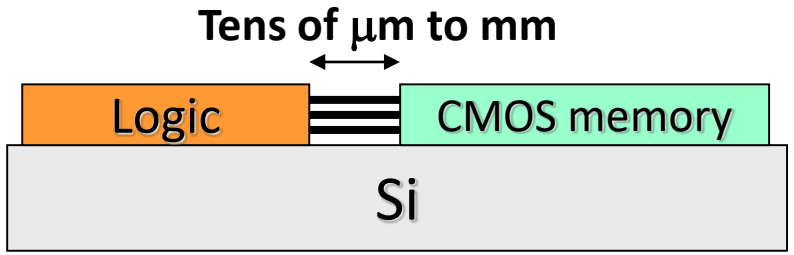
CMOS/magnetic integration for more efficient data transfer between memory and logic

Memory vs. CPU speed mismatch

Logic keeps waiting for data
+ large power consumption associated with transferring data between memory and logic blocks

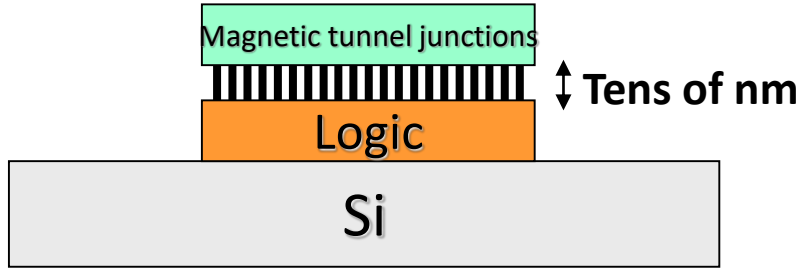


With silicon technology (CMOS) only:



-Slow communication between logic and memory
-few long interconnections
-Large dynamic consumption associated with data transfer
-complexity of interconnect paths
-large footprint on wafer

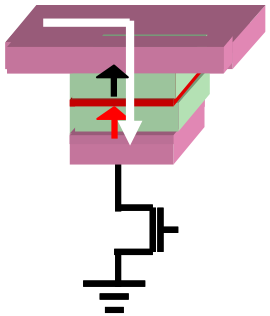
With hybrid silicon (CMOS)/magnetic:



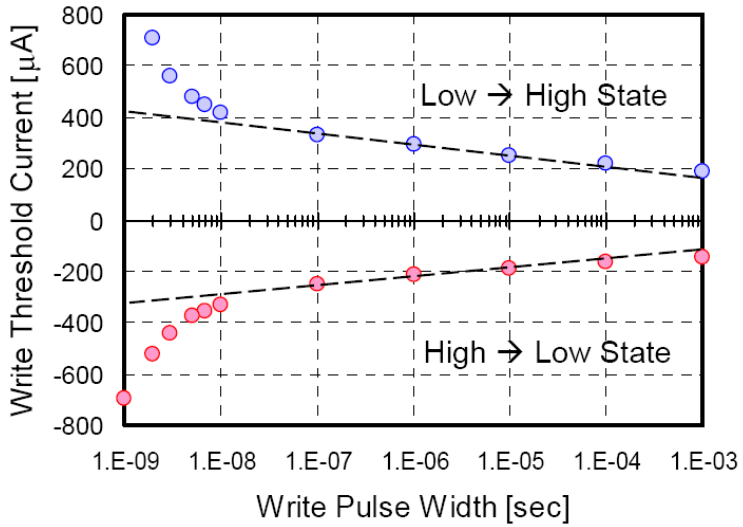
-Non-volatility in logic
-Reduced static and dynamic energy consumption
Bring logic inside the memory (« LOGIC IN MEMORY »)
-Fast communication between logic and memory
-Numerous short vias
-Simpler interconnect paths
-Smaller footprint on wafer

High speed memory : SOT-MRAM

With STT-MRAM, tradeoff between write speed and endurance :



M. Hosomi et al., IEDM 2005
Technical Digest, 459
Cell size : 115x155nm²



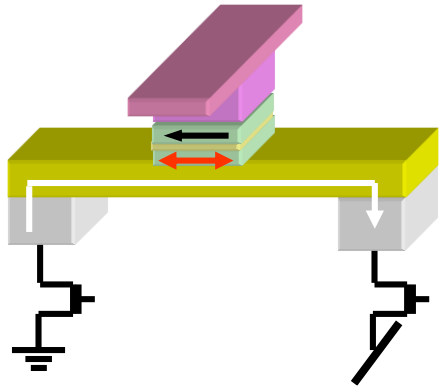
As often in microelectronics, going faster implies driving the system more strongly i.e. at higher voltages.

With 2 terminal devices, write endurance reduction ay high speed since write voltage approaches breakdown voltage.

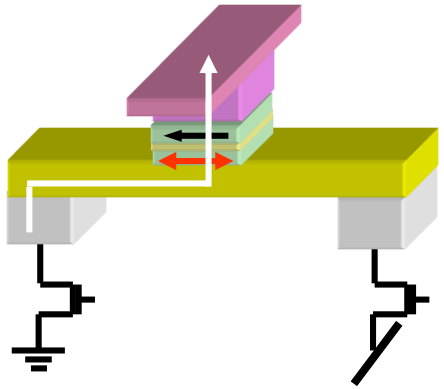
To circumvent this issue, 3 terminal devices written by SOT

M.Miron et al, Nature 476, 189 (2011)
L.Liu et al, Phys.Rev.Lett.106, 036601 (2011).

Write:



Read:

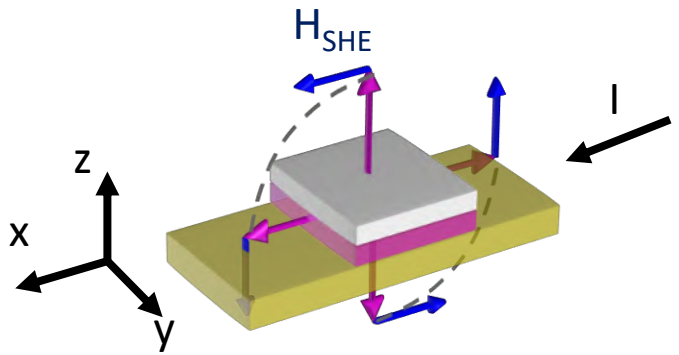


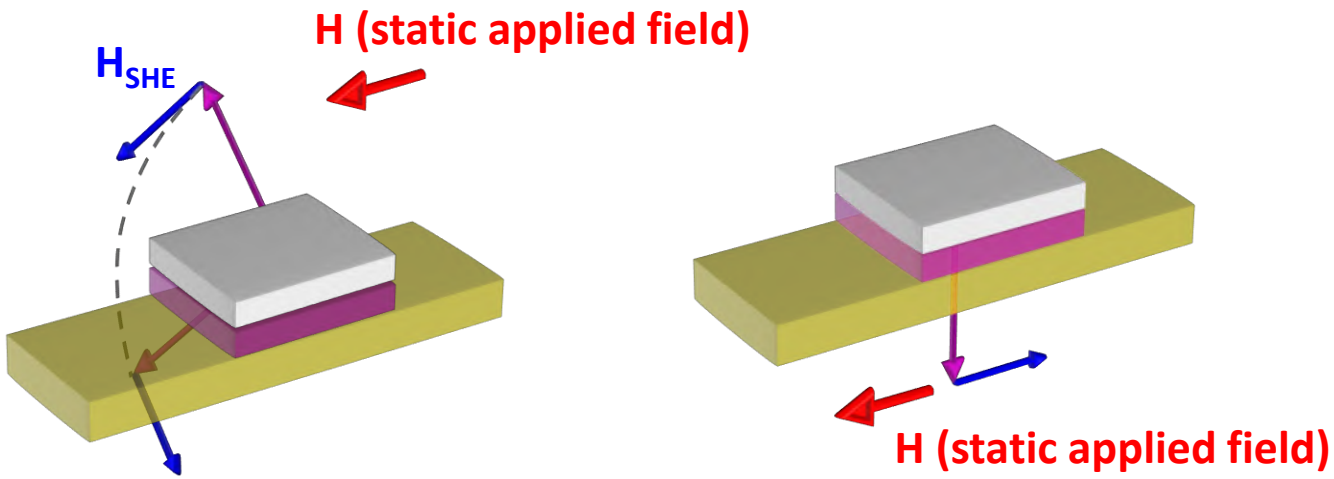
Separate write and read current paths

Spin-orbit-torque magnetization switching

Miron, et al., Nature, 476, 189 (2011)

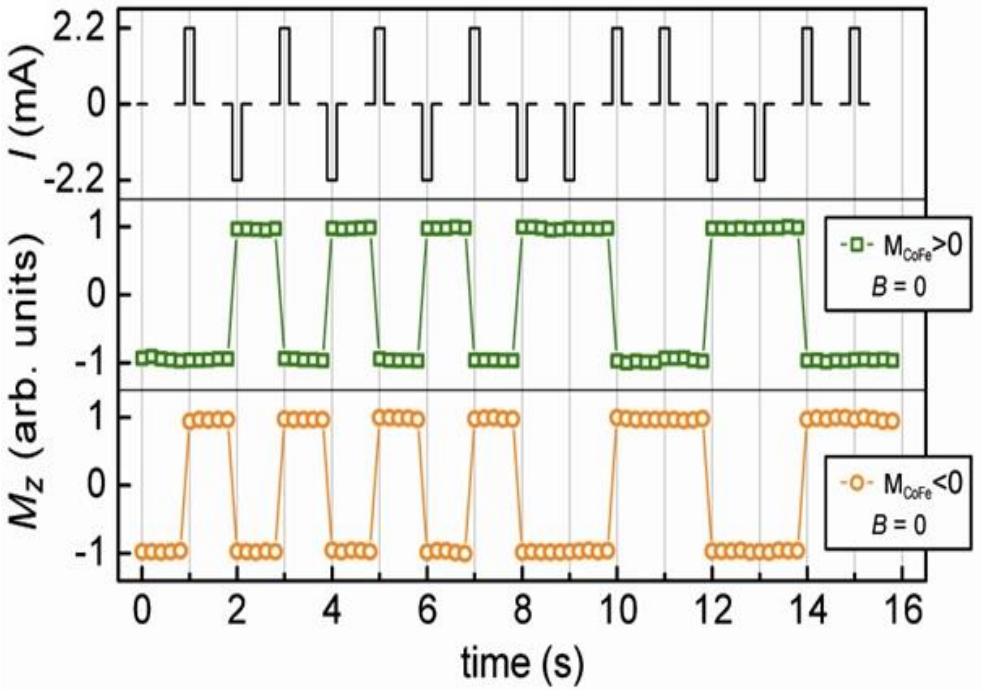
- When switching layer has out-of-plane anisotropy, **need to apply an external magnetic field** to break the symmetry between up and down states.



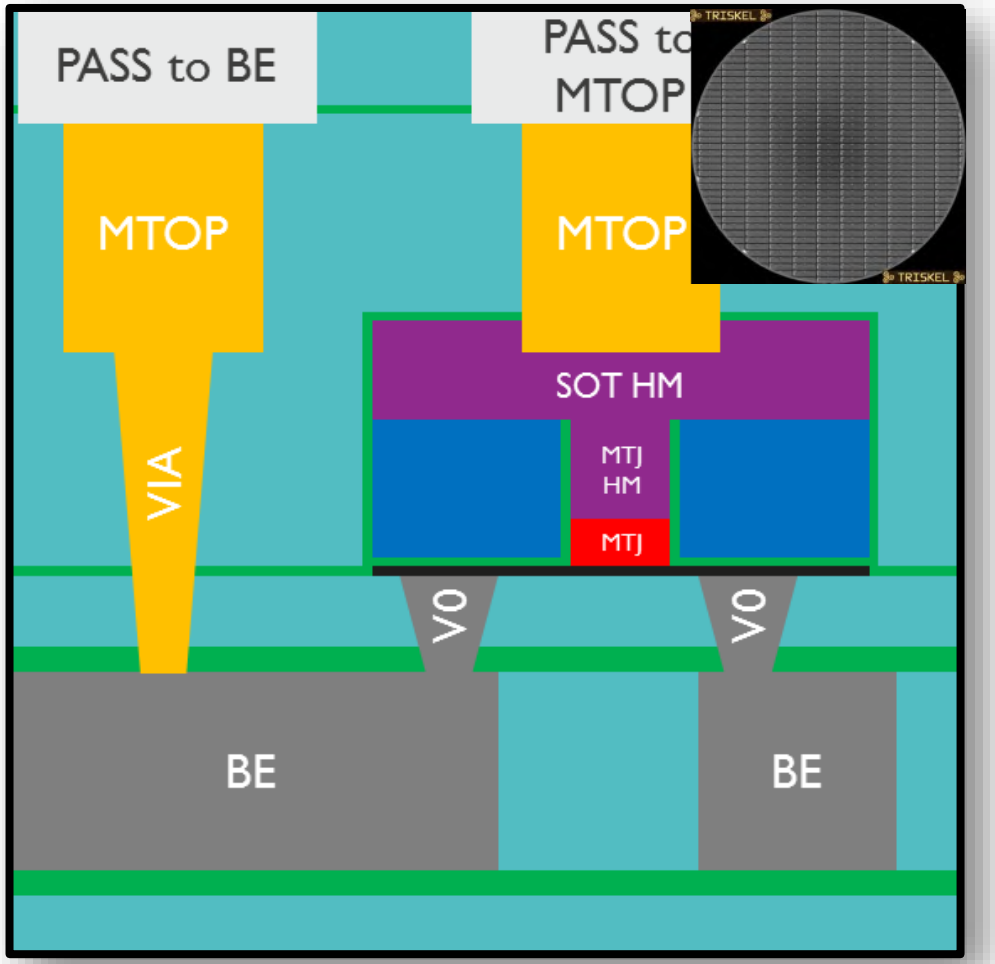


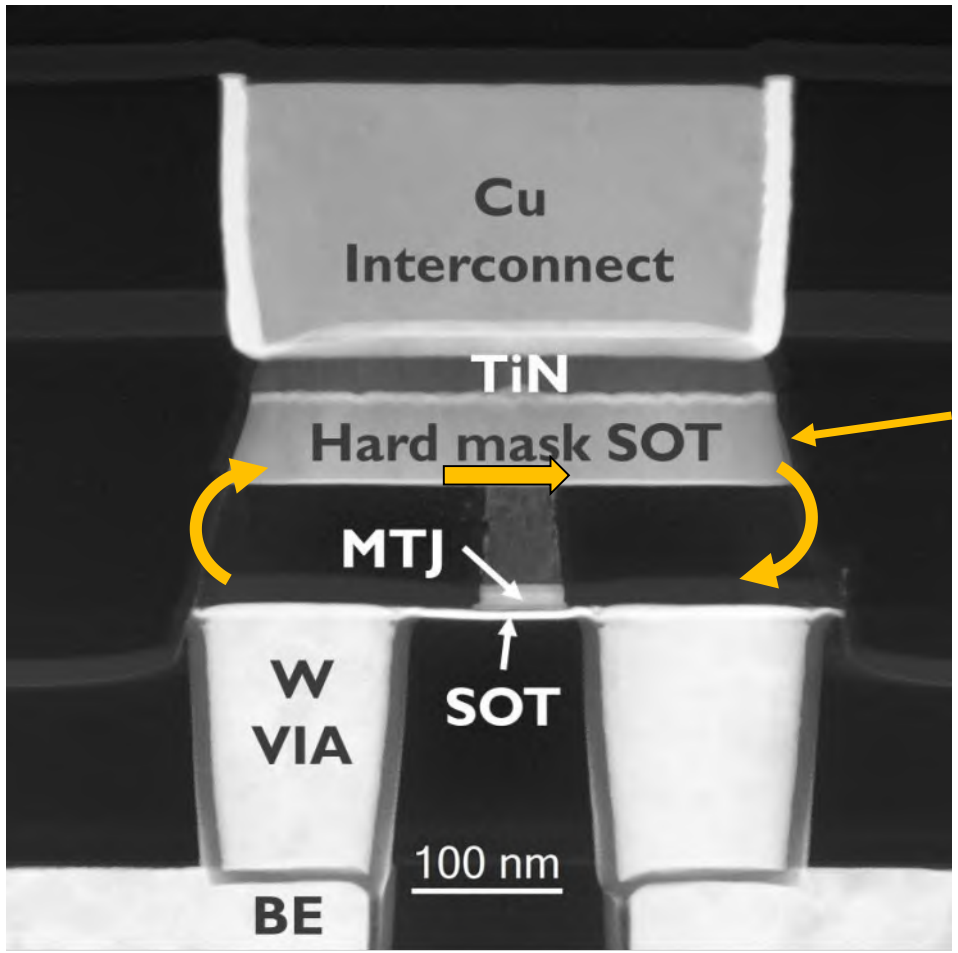
Up unstable

Down stable



First 300mm SOT-MRAM cell demonstration (IMEC)





magnetic

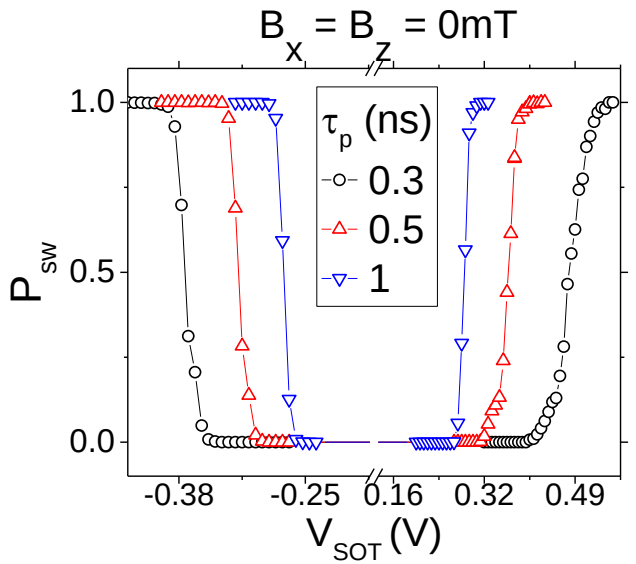
K. Garello et. al, VLSI Circuit Symposium, doi:10.1109/VLSIC.2018.8502269 (2018)

MTJ = 60nm SOT = 120*390nm²
Pitch: 260*540 nm²

Demonstrations of SOT-MRAM chips on 300mm wafers

imec

Manufacturable stand-alone SOT-MTJ with PMA technology and magnetic hard mask

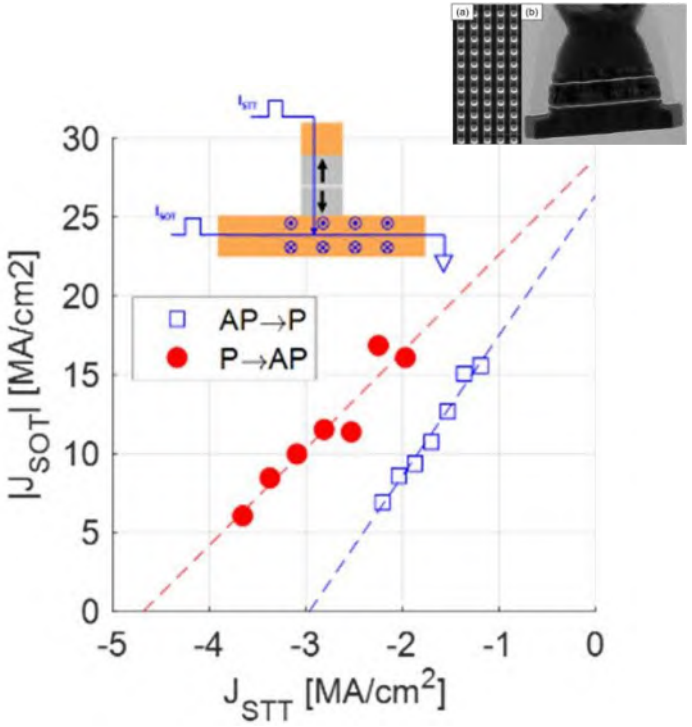


- Reliable sub-ns switching
- Sub-Volt operation

K. Garello et. al, VLSI Circuit Symposium, doi:10.23919/VLSIC.2019.8778100 (2019)

intel

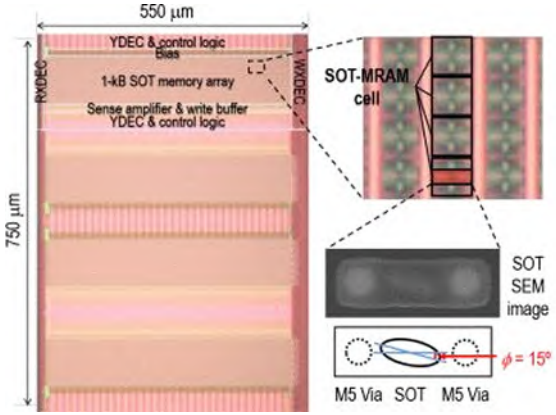
Hybrid SOT-STT with PMA technology



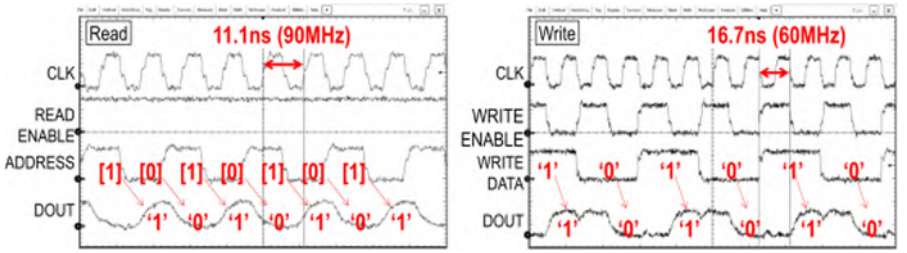
N. Sato et. al, INTEL, VLSI Technology Symposium 2020 doi:10.23919/VLSIC.2019.8778100 (2020)
M. Wang *et al.*, *Nat. Electron.*, vol. 1, no. 11, pp. 582–588, (2018)

TOHOKU UNIVERSITY

First integration of SOT-MRAM with CMOS (in-plane technology)



MOS tech. node	55-nm CMOS
SOT tech. node	88 nm x 315 nm elliptical shape
Supply voltage	1.2 V
Memory density	4 kB (128 cols. x 64 rows x 4)
Cell structure	2T-1SOT
Cell size	1.42 µm x 3.675 µm
Read frequency	90 MHz@1.2 V
Write frequency	60 MHz@1.2 V
Operation mode	8/16/24/32-bit write 32-bit read Synchronous read-during-write



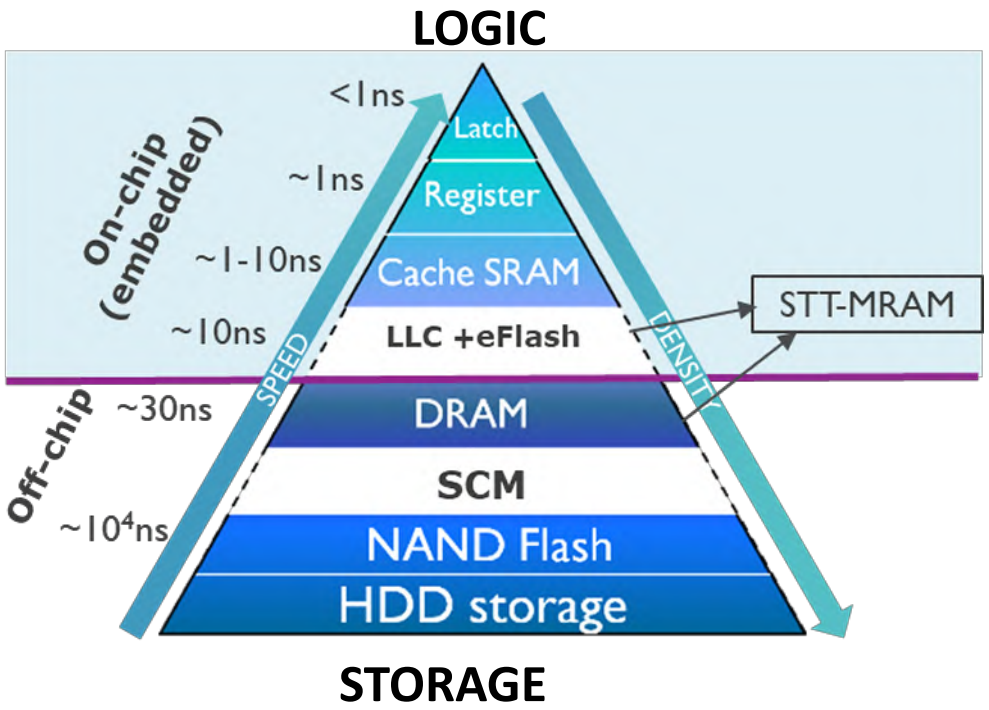
M. Natsui et. al, Tohoku, VLSI technology symposium 2020
DOI: 10.1109/VLSICircuits18222.2020.9162774

Near-memory or In-memory computing

Conventional computer architecture

Slow bandwidth between logic and memory
Logic operation much faster than data transfer + high power consumption associated with data transfer.

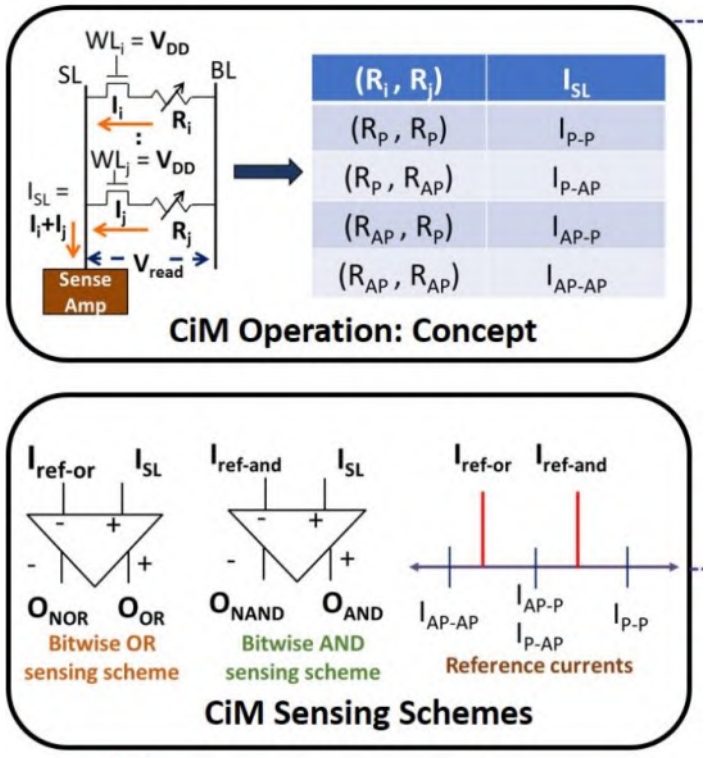
Issue partly addressed with memory hierarchy but not sufficiently



In-memory Computing

Perform logic operation inside the memory array

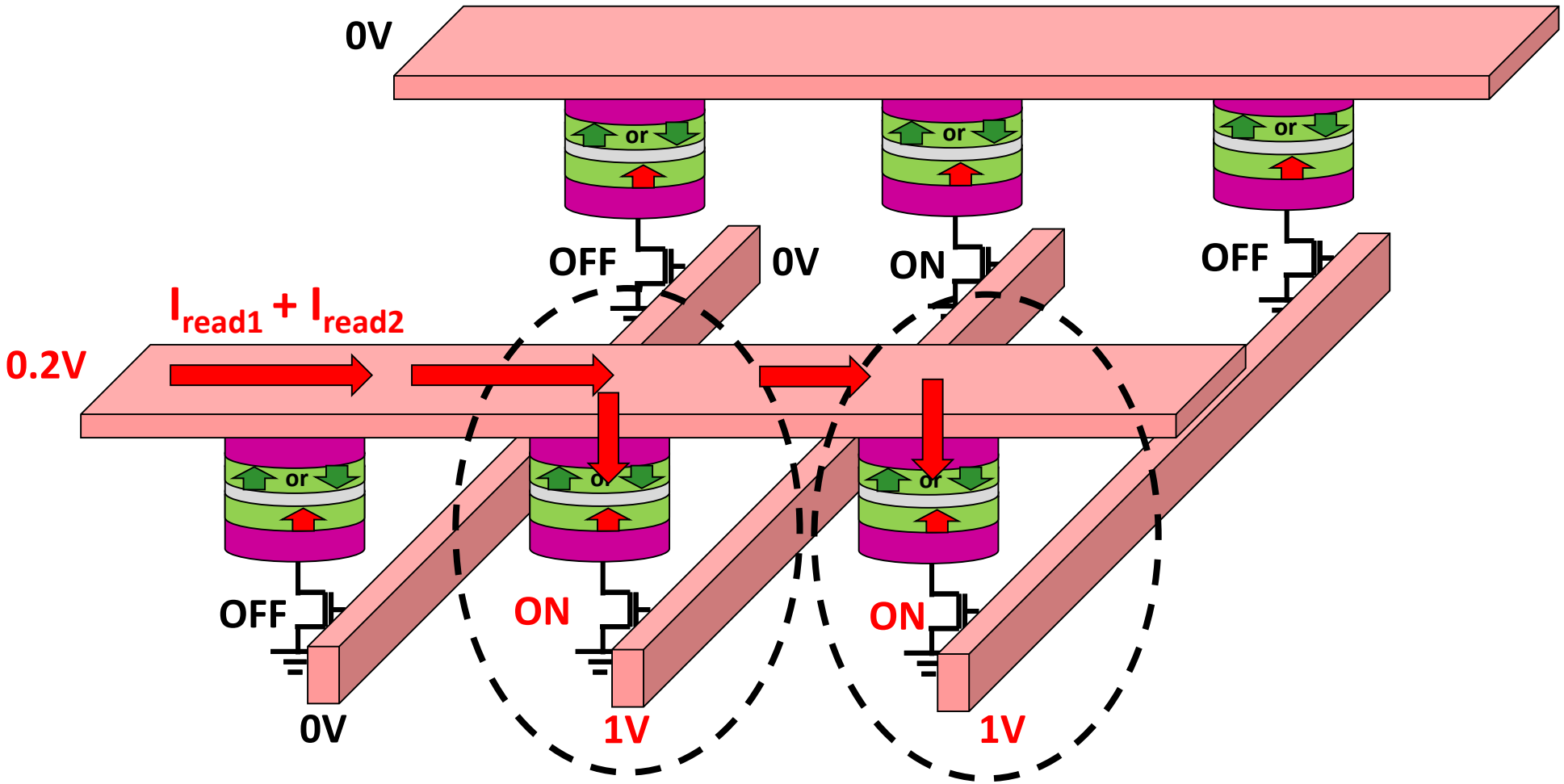
STT and SOT-MRAM well suited for this application thanks to their write speed and endurance



Activate several wordlines at the same time and compare the sum current to a threshold characteristic of the logic operation

Jain et al, Date18, DOI: 10.23919/DATE.2018.8342277

Perform logic operation directly in the memory without moving any data out-of the memory:

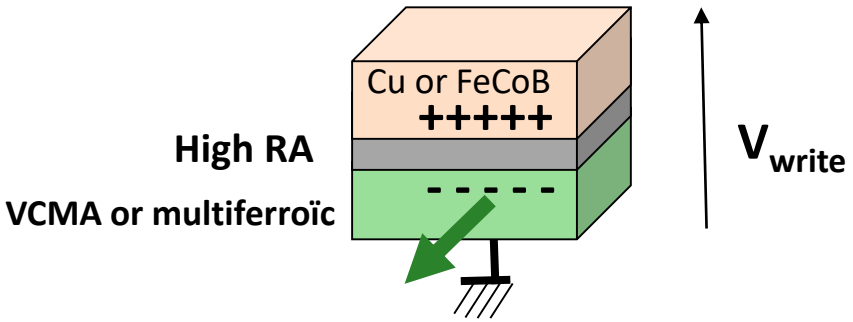


Towards ultralow power: Voltage controlled devices

- **Low power writing by voltage controlled magnetization switching :**

As long as required voltage to write below ~1V, $1/2CV^2 << RI^2\tau$

~aJ **~fJ**



- **Voltage Control of Magnetic Anisotropy (VCMA)**

  - **VCMA due to interfacial charge depletion/accumulation :**

    Relatively weak effect, β~10-100fJ/V/m

    Very fast change of Ks (sub-ps time scale)

  - **VCMA due to ionic migration** *U. Bauer et al, Nat. Mat. 14, 174 (2015)*

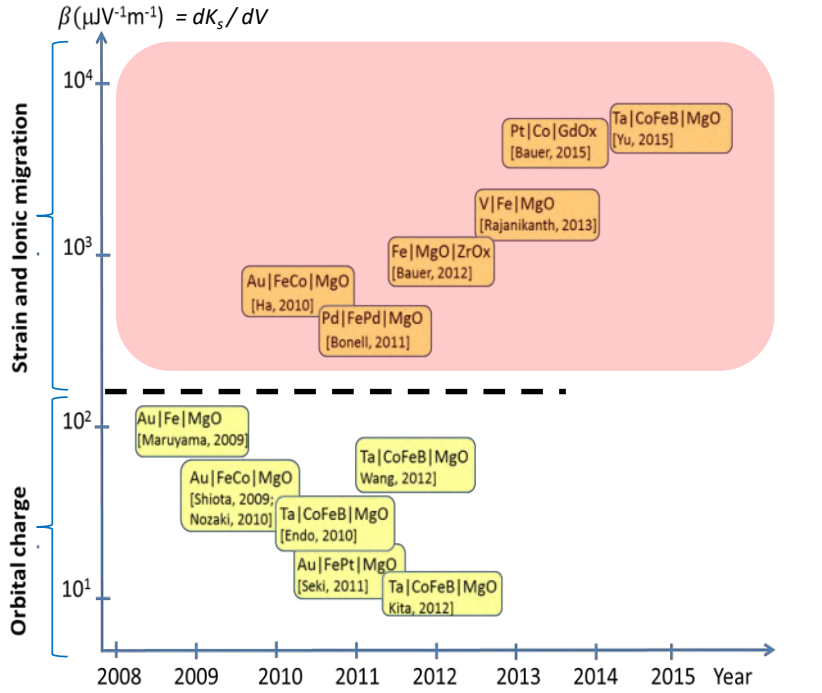
    Much larger amplitude β~200-10,000fJ/V/m

    Slower dynamics due to ionic motion (~µs-ms)

- **Multiferroïc materials** *: e.g. $BiFeO_3$ (Spaldin, Ramesh, Nat.Mat.18, 203(2019))*

- **Artificial combinations of piezo/magnetostrictive materials**

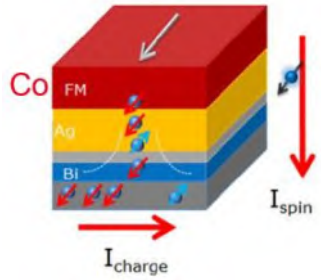
X.Liang et al, sensors, 20, 1532 (2020)



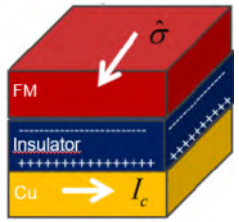
B.Dieny, M.Chshiev, Rev.Mod.Phys.89, 025008 (2017)

INTEL's MESO concept *(S. Manipatruni et al, arXiv:1512.05428 (Dec.2015); Nature Phys.14, 338 (2018))*

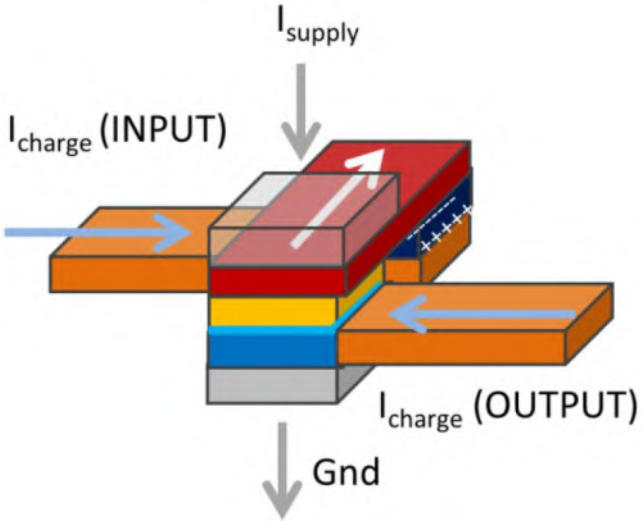
Spin to charge current conversion



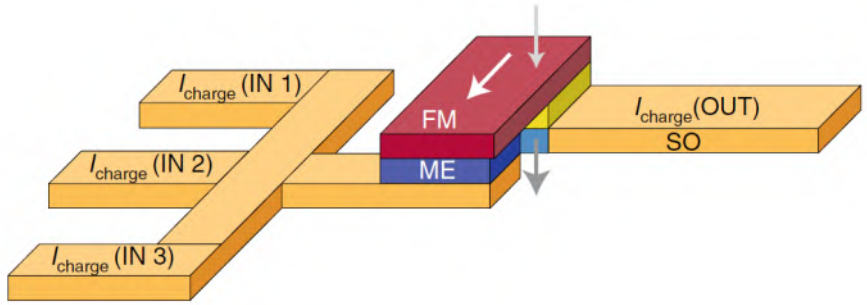
Voltage controlled writing

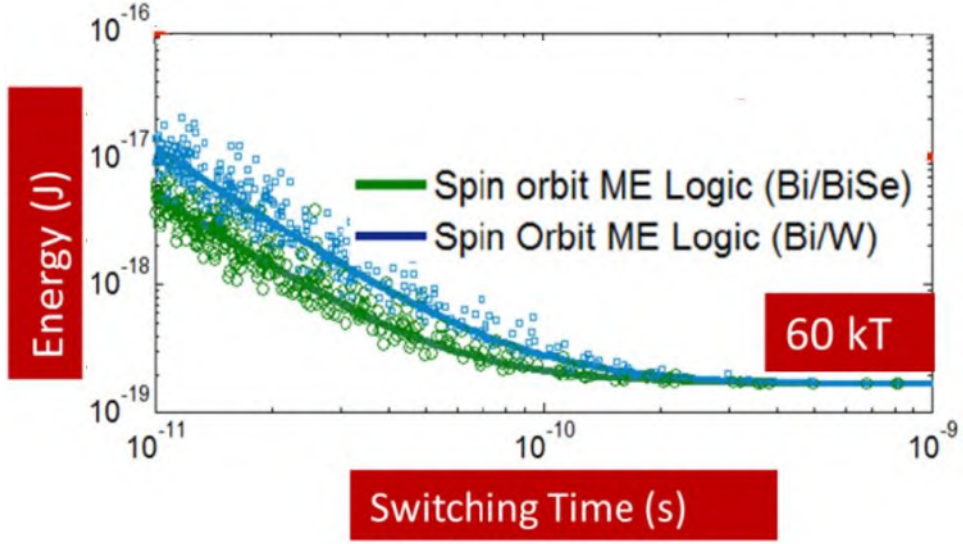


NOT gate



MAJORITY gate ➡ **Non-volatile logic with sub-aJ energy per write**





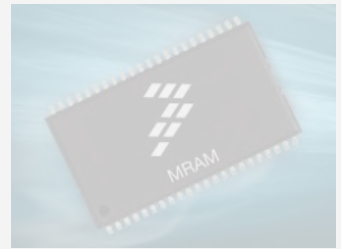
Very promising in terms of power consumption

but still lot of material and technological developments needed to make it work **(e.g. ability to switch magnetization with a few tens of mV)**

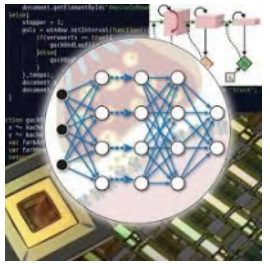
Spin-electronics can help !

- Data storage thanks to steadily increasing areal density on hard disk drives

- Non-volatile magnetic memories (MRAM) to reduce power consumption and speed up communication between logic and memory



- **Neuromorphic architecture to improve computing efficiency for specific applications**



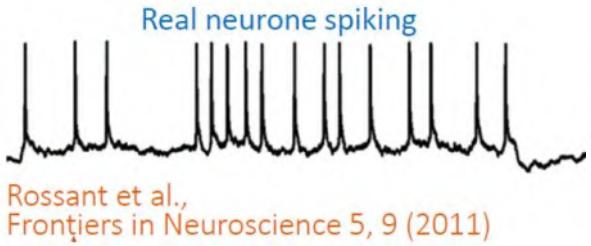
Neuromorphic electronics

Brain 20 W

- Low power
- Non-linear, stochastic

High-performance computing 10 MW

- High power
- Deterministic

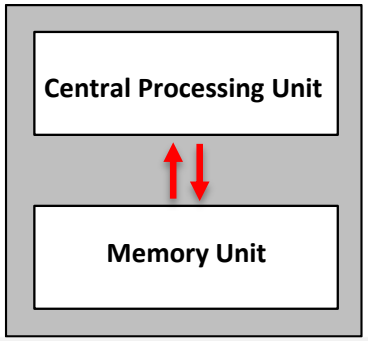


Rossant et al.,
Frontiers in Neuroscience 5, 9 (2011)

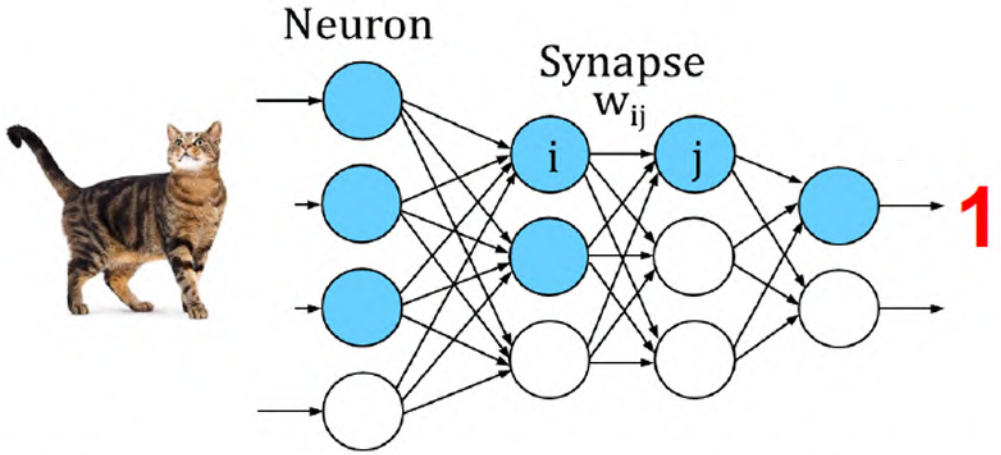
Brain :

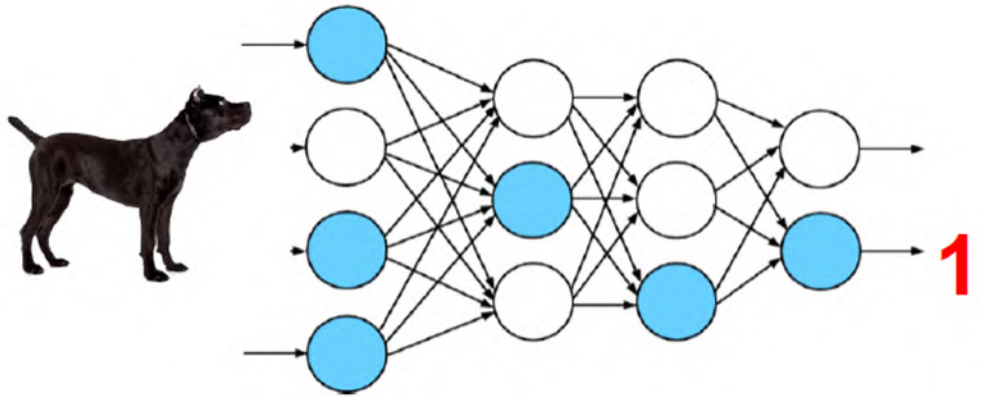
- **Analog,**
- **Memory and processing are intimately mixed**
- **Massively parallelized processing**
- **Time scale per operation ~ ms**

Computer : Von-Neuman architecture



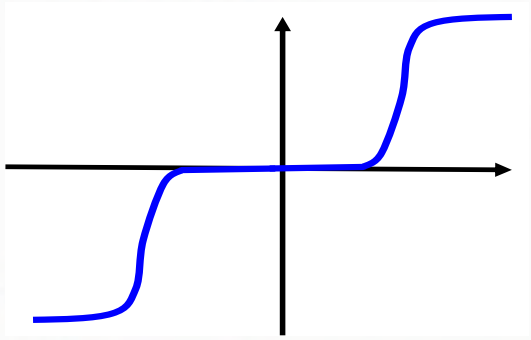
- **Digital,**
- **memory and processing are separated,**
- **sequencial processing in CPU,**
- **parallel processing in GPU**
- **Time scale per operation ~ns**





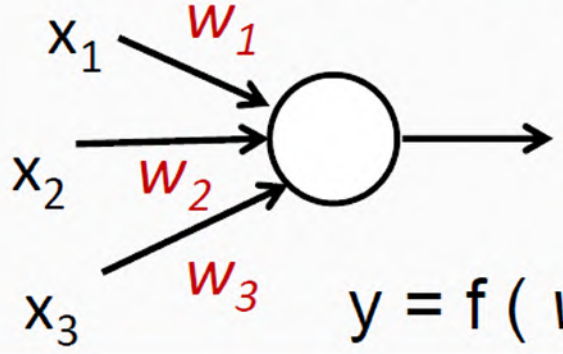
Neurons

- Non-linear



Synapses

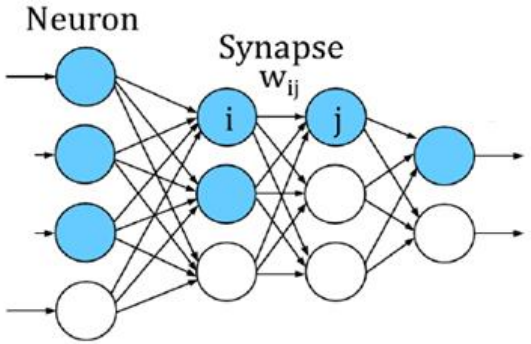
- Analog valves (weighs w)



$$y = f (w_1 x_1 + w_2 x_2 + w_3 x_3)$$

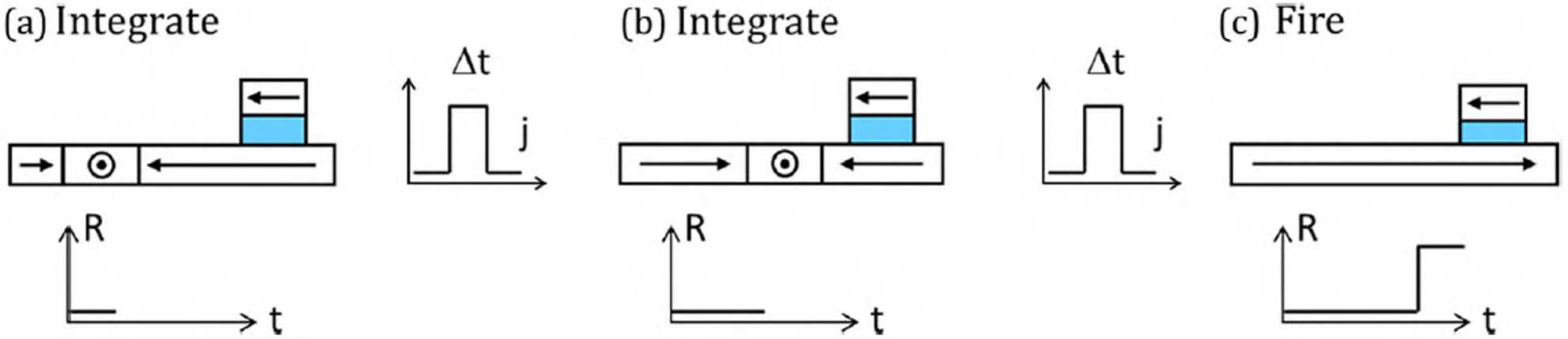
- **Ingredients for neural networks: non-linearity, memory and plasticity**

Neuron : Integrates the input signals up to a certain threshold above which an electrical pulse is generated and sent towards the next interconnecting synapses



$I_{input} > I_{switch}$

Example : artificial neuron based on current induced domain wall propagation



After firing the neuron must be reset in (a)

J.Grollier et al, PIEEE 104, 2024 (2016)

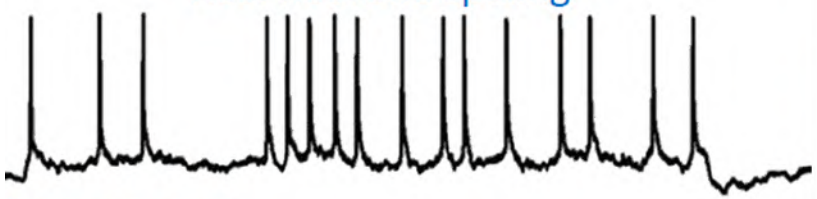
Using spin-torque nano-oscillators and stochastic MTJ for neuromorphic computing

Assets of spintronics hardware components for artificial Intelligence (AI)

- Intrinsically hysteretic and non-linear
- Much lower power and footprint than dedicated CMOS AI

NB: weakness = small gain

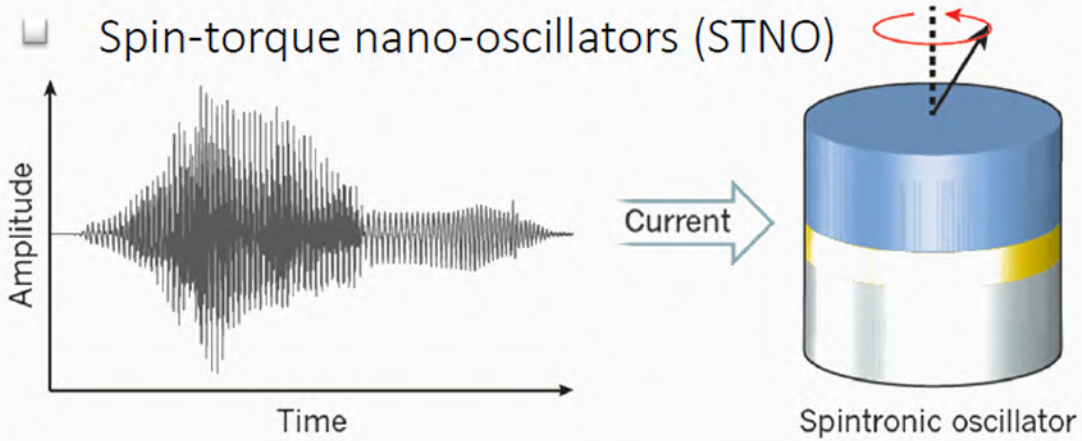
Real neurone spiking



Rossant et al.,
Frontiers in Neuroscience 5, 9 (2011)

Non-linearity

- Spin-torque nano-oscillators (STNO)

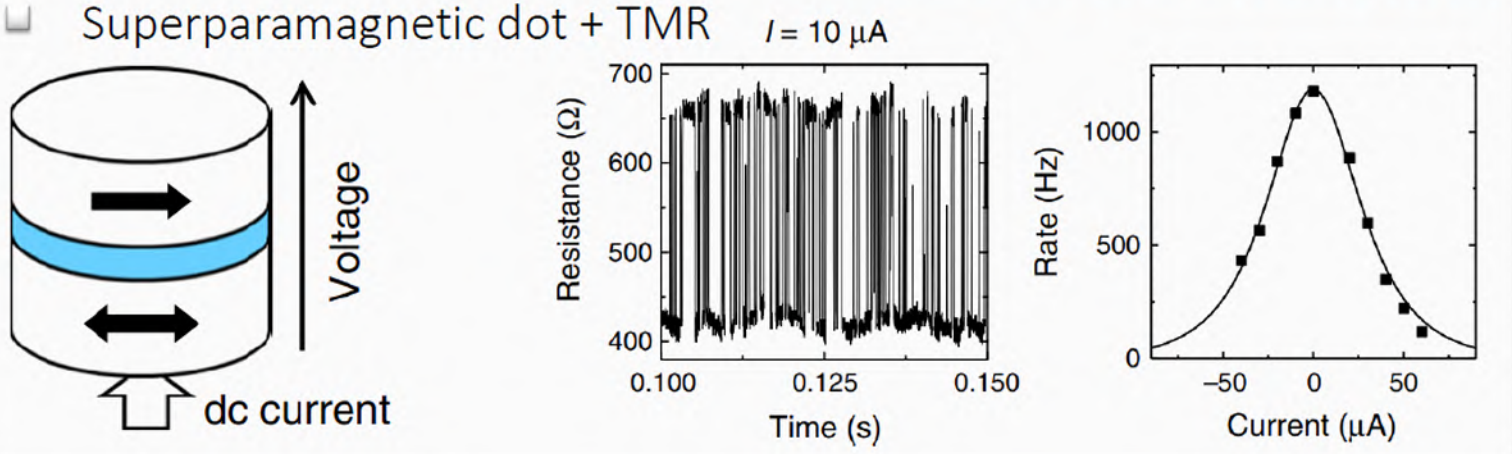


J. Torrejon et al,
Nature 547, 428 (2017)

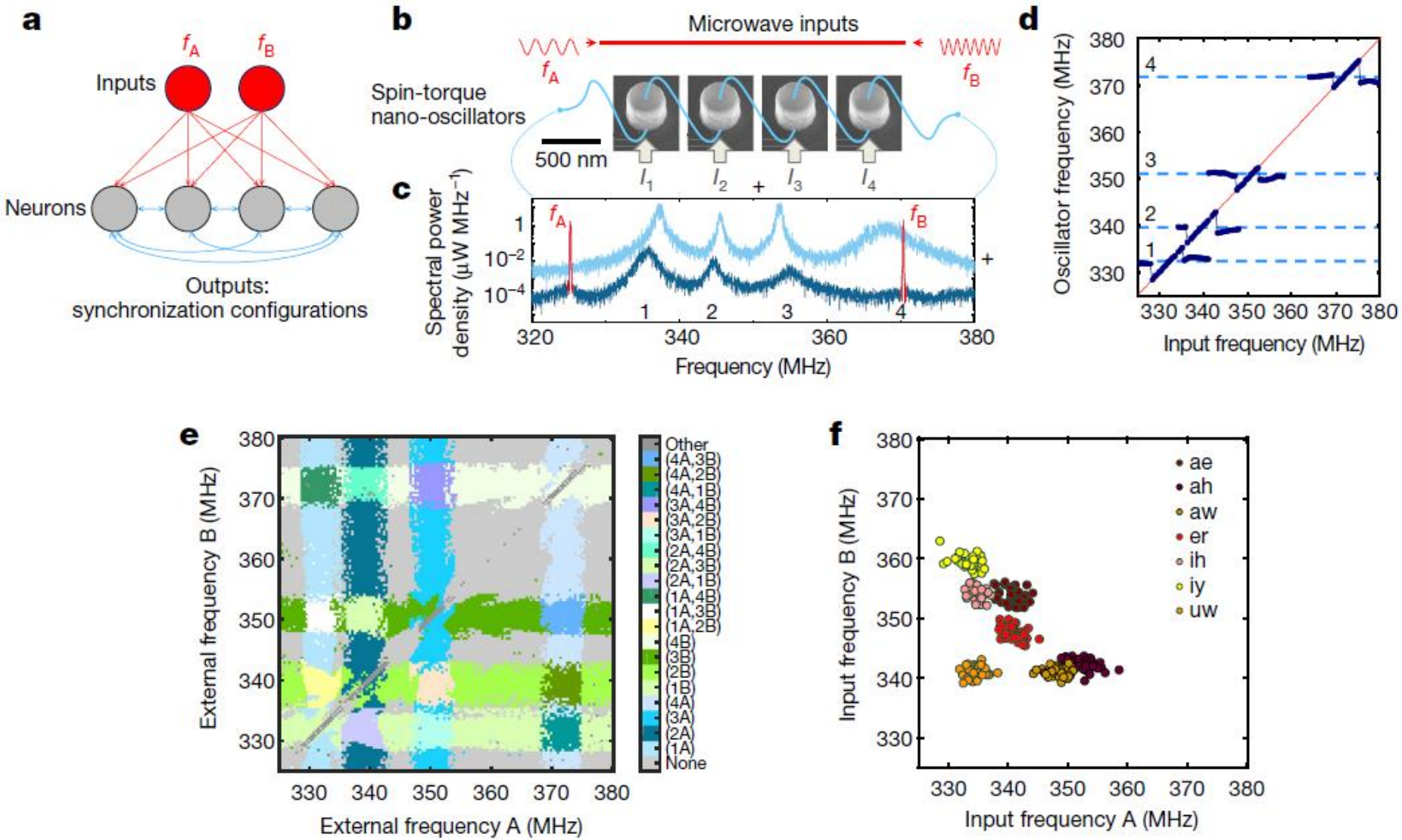
Stochasticity

A. Mizrahi, Nat. Comm. 9, 1533 (2018)

- Superparamagnetic dot + TMR



Example: vowel recognition from the synchronization pattern of an array of 4 nano-oscillators



M.Romera et al, Nature, 563 (2018)

CONCLUSION

- **Hard disk drives technology ,** a “Formule 1+++” technology which works ! Despite competition with SDD, will still be commercialized for quite some time considering the exponentially growing amount of data to be stored.

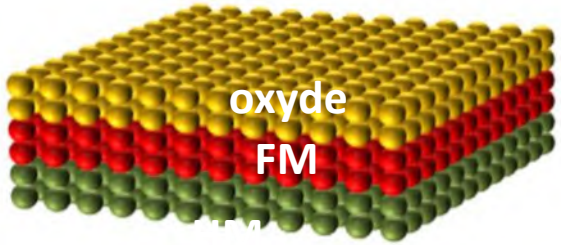
- **STT-MRAM constitutes the 2nd major application of spintronics** after HDD and magnetic field sensors

- **STT-MRAM** have **now entered in volume production** (Samsung, TSMC, Global Foundries, INTEL).
  - **Replacement of embedded Flash** (much fewer masks required for fabrication of STT-MRAM (3) vs >15 for eFLASH).
  - **Last level Cache** and persistent memory application (much smaller footprint than SRAM + non-volatility).
    However, may be better addressed by SOT-MRAM.

- The launching of MRAM volume production marks the **acceptance of this hybrid CMOS/magnetic technology by microelectronics industry**. Will greatly facilitate the industrialization of future “bright ideas” of spintronic devices

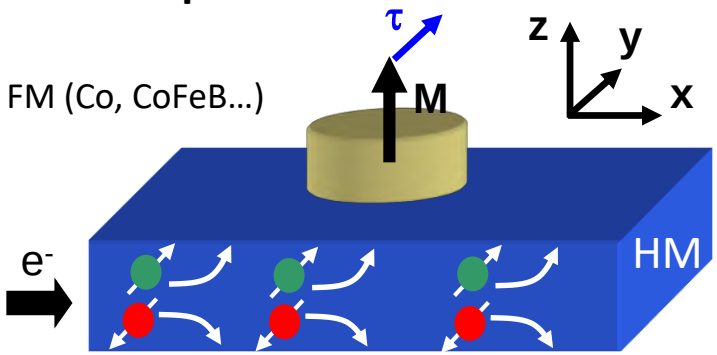
- Further applications of MRAM foreseen in the field of **AI, In-memory computing, low power electronics, IoT, High Performance Computing (HPC), cryoelectronics**…

Magnetization reversal by spin-orbit-torque in MTJ electrode with in-plane current



→ Heavy metal with **high atomic SO coupling** (Ta, Pt, W, high SO alloy)
→ **Structural inversion asymmetry**
→ Atomically **thin** ferromagnetic films

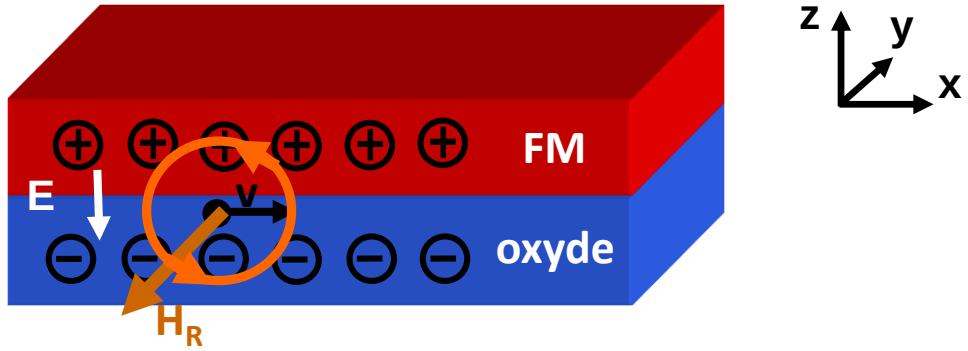
Bulk : Spin Hall Effect



→ Vertical spin current with transverse polarisation $\mathbf{u}_y$. Spin Hall angle $J_s=\theta_{SH}\,J$
→ **Damping like torque** $\tau\sim\theta_{SH}\,J\,m\times(m\times u_y)$

📖 *Liu et al., (Science 2012) , Liu et. al (2012)*
📖 *Kim, Hayashi et al. Nature Mater. (2013)*
📖 *X. Fan, J. Xiao et. al, NatCom (2014)*

Interface: Rashba Spin Orbit coupling



$H_R \sim \langle v\rangle \times E \sim J\times E \sim JEu_y$

Field like torque $\tau\sim Jmxu_y$

📖 *Manchon et al., PRB 78, 212405 (2008)*
📖 *Hane et. al .PRB (2013)*
📖 *H. Yang et. al,PRL (2014)*