Magnetic memories from a broad IT, materials, and physics perspectives

T. Jungwirth Institute of Physics, Czech Academy of Sciences University of Nottingham, United Kingdom jungw@fzu.cz

Recording & computers
 Conventional & neuromorphic computing
 Non-CMOS materials and devices
 Physical principles of operation of magnetic devices

Recording



Mechanical gramophone 1870's



Electro-magnetic wire recorder 1880's

Boom, bust, boom,...

Recording & computers

sound & video



1930's Tape recorder

1980's Compact disk (100sMB-GBs)

- Analog to digital
- Phase-change
- Optical

1990's - Spintronic



Sony/IBM tape (330TB)

Storage



Seagate HDD (16TB)



Everspin MRAM (1Gb)

data



1950's Magnetic hard disk (MBs) & core memory (kbs)

Back-up

- Internet (PC & cloud IT)



- Internet of Things (edge IT)



Recording & computers

- Big data

Zettabytes of data created

44*

50

2013

2016

2020

2025

4.4

16

Back-up

Sony/IBM tape (330TB)

Storage



Seagate HDD (16TB)

 $ZB = 10^9 TB = 10^9 people x 1TB mobile phone$

100

Nearly 20 per cent (about 32ZB) of the data created will be critical to daily life and the smooth running of government and businesses.

163*

200

150



International technology roadmap for semiconductors





Transistor 1947 Integrated circuit 1958

International technology roadmap for semiconductors





Transistor 1947 Integrated circuit 1958



1. Recording & computers

- 2. Conventional & neuromorphic computing
- 3. Non-CMOS devices and materials
- 4. Physical principles of operation of magnetic devices

Let's racap

		- von Neumann
	do differently	Revisit the architecture to tackle the bottleneck
	uo uijjerentiy	- Analog to digital
		Revisit the noise vs. complexity trade-off
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		- Spintronic
		- Phase-change
S		Exploit full potential of non-CMOS devices
	do more	
		- Optical
		Explore speed and energy efficiency limits



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Neuromorphic architecture





Brain: Massively **parallel** neural network architecture connecting 100billion low-power **computing and memory** elements

cf. Samsung 1TB Flash-SSD for smart phones with 2 trillion transistors on a chip



Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)



https://cloud.google.com/blog/products/ai-machine-learning/what-makes-tpus-fine-tuned-for-deep-learning

Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)



Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)



1.1 Off-shelf

General purpose CPU (Intel,...)

1 or few big cores



OUTPUT

Serial & von Neumann bottleneck

Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)



1.1 Off-shelf

General purpose GPU (NVIDIA, AMD)

2,000 medium cores

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OUTPUT

Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)



Highly parallel & tackles von Neumann bottleneck

Mass applications – Google Brain (2012 – image recognition, 2016 – language translation)

OUTPUT



Highly parallel & tackles von Neumann bottleneck

Still mostly in research phase

- Short-term: Save bandwidth & energy



Still mostly in research phase

- Long term: Help understand neuroscience, develop General Artificial Intelligence



Spiking time dependent plasticity of synapse ("neurons that fire together wire together")





Gerstner & Kistler, Spiking Neuron Models, Cambridge University Press (2002)

Kurenkov et al. Adv. Mater. 31, 1900636 (2019)

2.1 Off-shelf based

FPGA DeepSouth (Sydney Univ.)

Mobile CPU SpiNNaker (Manchester Univ.)

Thakur et al. Frontiers in Neuroscience 12, 891(2018)

2.2 Custom-designed CMOS

Individual circuit components mimic bio-neuron structure and functions





2.2 Custom-designed CMOS

Individual circuit components mimic bio-neuron structure and functions



2.2.1 CMOS digital TrueNorth (IBM) – 1M neurons Low-power execution Learning done externally Merolla et al. et Science 345, 668 (2014)

Loihi (Intel) – 100k neurons Includes learning



2.2.2 CMOS mixed digital/analog
Neurogrid (Stanford) – 60k neurons
Dynap-SEL (Zurich Univ.) – 1000 neurons
HICANN (Heidelberg Univ.) – 500 neurons
Benjamin et al. Proceedings of the IEEE 102, 699 (2014)
Digital communication
Analog neuron
Analog synapse with weights stored in digital RAM



Reviews:

Thakur et al. Frontiers in Neuroscience 12, 891(2018) Yu (ed.), Neuro-inspired Computing Using Resistive Synaptic Devices, Springer (2017) Burr et al. Adv. Phys. X 2, 89 (2017)

3. Mixed CMOS/non-CMOS

3.1 Analog memristive synapse CBRAM (Michigan Univ.) Jo et al. Nano Lett., 10, 1297 (2010) **RRAM** (Pohang Univ.) Moon et al. Nanotechnology 25, 495204 (2014) **PCRAM** (IBM) Eryilmaz et al. Frontiers in Neuroscience 8, 205(2014) **FRAM** (Panasonic) Ueda et al. PLOS ONE 9, e112659 (2014) **MRAM** (Tohoku Univ.) Borders et al. Appl. Phys. Exp. 10, 013007 (2017) with SW or CMOS HW neurons

Ferromagnetic domains



MRAM

Defects in insulator



CBRAM/RRAM





FRAM

3.2 Analog memristive synapse & neuron Analog PCRAM (IBM)

Pantazi et al. Nanotechnology 27, 355205 (2016)

Spiking NN

Analog MRAM (Tohoku Univ.)

Kurenkov et al. Adv. Mater. 31, 1900636 (2019)

Analog AFMEM (Prague/Nottingham/Mainz/...)

Discrete synapse or neuron

Kaspar et al. preprint (2019)

Antiferromagnetic domains



Reviews: Thakur et al. Frontiers in Neuroscience 12, 891(2018) Yu (ed.), Neuro-inspired Computing Using Resistive Synaptic Devices, Springer (2017) Burr et al. Adv. Phys. X 2, 89 (2017)

AFMEM

Revi

3. Mixed CMOS/non-CMOS

3.3 Analog memristive weighted-sum (dot product) array RRAM passive array (UCSB) *Prezioso et al. Nature 521, 61 (2015)* **RRAM 1T1R array (**Mass. Univ., HP) *Hu et al. Nature Elec. 1, 52 (2018)*









Kirchhoff's rule

Non-CMOS vs. CMOS for neuromorphics

Digital artificial neural networks for cloud IT Compete with Google



Analog spiking neural devices for edge IoT More realistic R&D start





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Non-CMOS memristive materials

CoFeB IrMn																				
MRAM	Metal		PCRAM Metalloid										CBRAM, RRAM Nonmet							
	H AFMEM											V				~	He			
	Li	Be											В	С	N	0	F	Ne		
	Na	Mg											Al	Si	Р	S	Cl	Ar		
	к	Са	Sc	Ti	V	Cr	Mn	Fe	Со	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr		
	Rb	Sr	Υ	Zr	Nb	Мо	Тс	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Те	Т	Xe		
	Cs	Ва	La-Lu	Hf	Та	W	Re	Os	lr	Pt	Au	Hg	ΤI	Pb	Bi	Ро	At	Rn		
	Fr	Ra	Ac-Lr																	

La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Тb	Dy	Но	Er	Tm	Yb	Lu
Ac	Th	Ра	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Conductive-Bridging RAM

Adesto EEPROM CBRAM 1µs & 512kb





Bipolar switching Micron/Sony 16Gb, 10µs prototype binary CBRAM

> Yu (ed.), Neuro-inspired Computing Using Resistive Synaptic Devices, Springer (2017) Burr et al. Adv. Phys. X 2, 89 (2017)

Analog synapse 0.8 Ag/Si(~1-10 nm) 300µs-pulse 0.7 D Current (100 nA) 0.6 0.5 0.4 0.3 20 40 60 80 0 Pulse # (after 1.0 x 10⁷ cycles)

Jo et al. Nano Lett., 10, 1297 (2010)



Resistive RAM





Moon et al. Nanotechnology 25, 495204 (2014)



Phase change RAM







Phase change RAM

Phase change RAM

Zhong et al. Phys. Stat. Sol. RRL 9, 414 (2015)

Borders et al. Appl. Phys. Exp. 10, 013007 (2017)

UDP

Ethernet PHY

PC

Ethernet PHY

FPGA Development Board

Ferromagnetic domains

Kurenkov et al. Adv. Mater. 31, 1900636 (2019)

Single 100 fs pulse of ~1-10s mJ/cm² and reversal time ~10s ps

Ostler et al. Nat. Comm. 3, 666 (2012) Stupakiewicz et al. Nature 542, 71 (2017)