From physics to products

From MRAM to MLU and beyond memory

Magnetic Random Access Memory

Magnetic Logic Unit

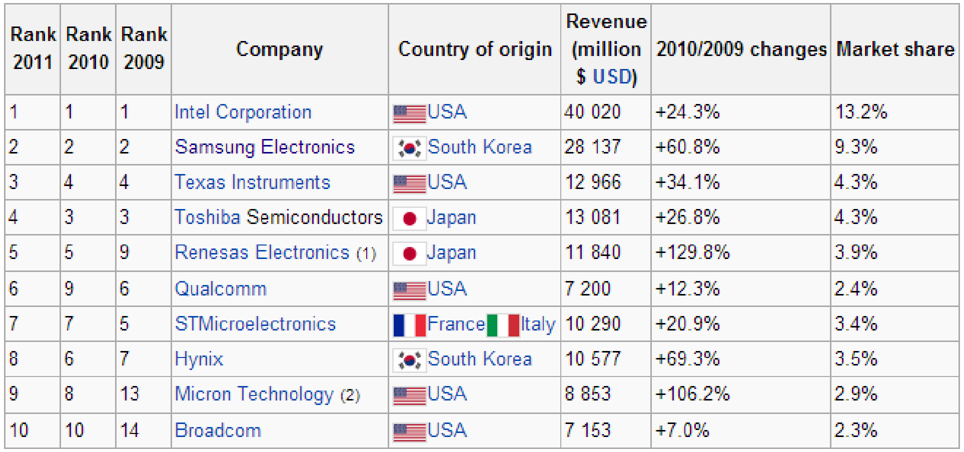
Lucien Lombard
Crocus-Technology

Overview

- **1 - The semiconductor industry**
- **2 - Crocus-Technology**
- **3 - MRAM Technology**
- **4 - From the Lab to the Fab challenges of industrial products**
- **5 - From TAS to MLU**
- **6 - Product developments**
- **7 - Conclusion**

The semiconductor industry

Assembly of companies engaged in the design and fabrication of integrated circuit.



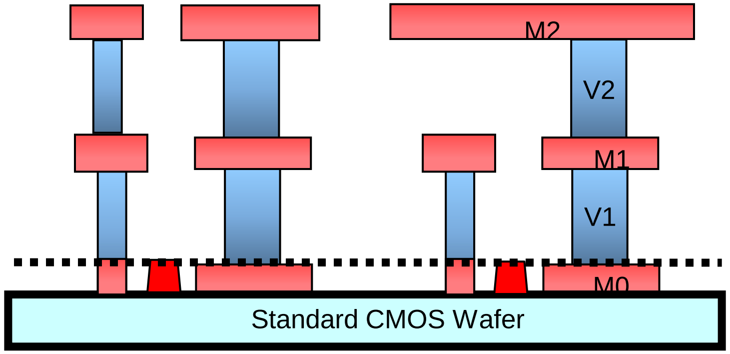
Rank 2011	Rank 2010	Rank 2009	Company	Country of origin	Revenue (million $ USD)	2010/2009 changes	Market share
1	1	1	Intel Corporation	USA	40 020	+24.3%	13.2%
2	2	2	Samsung Electronics	South Korea	28 137	+60.8%	9.3%
3	4	4	Texas Instruments	USA	12 966	+34.1%	4.3%
4	3	3	Toshiba Semiconductors	Japan	13 081	+26.8%	4.3%
5	5	9	Renesas Electronics (1)	Japan	11 840	+129.8%	3.9%
6	9	6	Qualcomm	USA	7 200	+12.3%	2.4%
7	7	5	STMicroelectronics	France Italy	10 290	+20.9%	3.4%
8	6	7	Hynix	South Korea	10 577	+69.3%	3.5%
9	8	13	Micron Technology (2)	USA	8 853	+106.2%	2.9%
10	10	14	Broadcom	USA	7 153	+7.0%	2.3%

Source : iSuppli Corporation supplied rankings for 2010 (Semiconductor foundries are excluded)

Industry dominated by US, Japan and South Korea

- Generate ~$300 billions revenue (year2010).
- Formed around 1960.
- Principle : use semiconductor material to realise transistor based integrated circuits.

CPU, Memory, amplifiers,…



- What bring semiconductor devices :
  - Low Power comsumption and power dissipation
  - High reliability
  - Small size

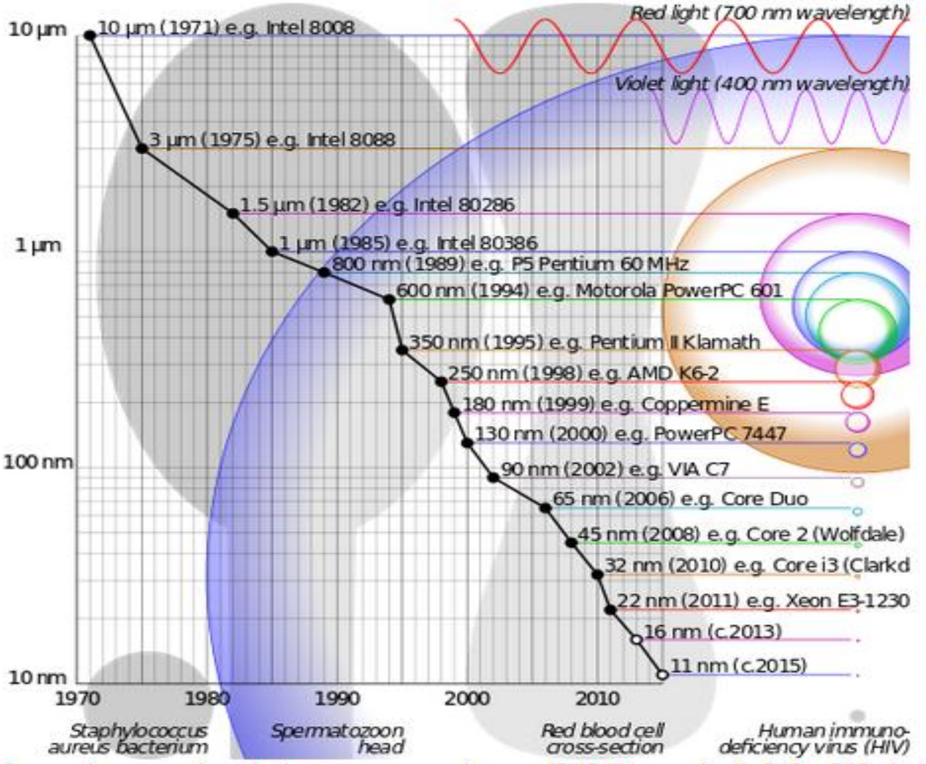
→ **allow IC miniaturization**

Note : IC = Integrated Circuit
CMOS = Complementary Metal-Oxide Semi-conductor

The semiconductor industry

An Industry organized to follow a Very Agressive Roadmap over the last 40 years!!

→ higher performances at reduced cost to increase profits



- Technology node shrinked from 10µm to 10nm
- Wafer size increased from 50mm to 300mm (450mm wafers in a few years)

How to continue this road map? What can be done beyond CMOS?

For futher reference see the International Technology Roadmap for Semiconductors @ http://www.itrs.net

Key Milestones
Partnership with Leaders

2006/2008
- Crocus funded: CEA/LETI/Spintec
- MRAM development: SVTC

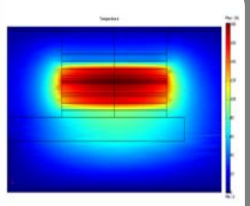
2009
- Manufacturing - Tower Jazz @ 130nm

2010/2012
- Invent MLU: MIP – Logic
- $250M JV: CNE @ 90nm-65nm-45nm
- JDA with IBM: MLU deployment

Business development
- with Morpho: Smartcard
- with Inside secure
- with SMIC: CMOS supply

Corporate Profile

- Powerful Ecosystem



Technology:

Magnetic Logic Unit (MLU$^{\text{TM}}$)

> 150 patents

> Memory blocks, Logic, Analog

Product Focus: MCU

Smartcards/Secure MCU

High temperature

Smart sensors amplifiers

NV-SRAM

Investors:

$125M cash raised

Committed Syndicate

R&D Partners:

IBM JDA – Yorktown

CEA - Grenoble

Manufacturing Partners:

Crocus Nano Electronics

Tower Jazz

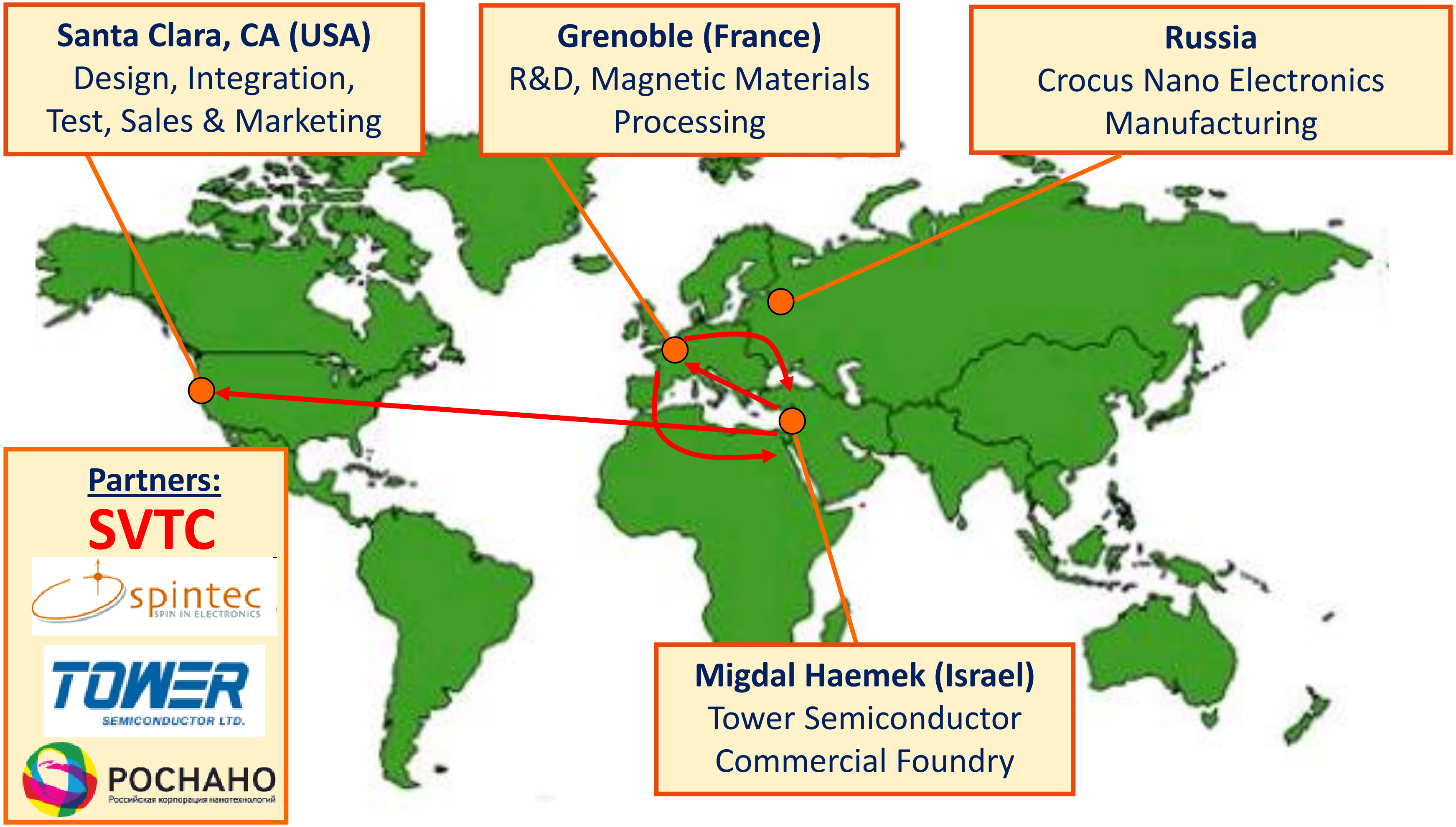
SMIC

Strong team:

50 Employees

»200 Associated persons

Operations



Santa Clara, CA (USA)
Design, Integration,
Test, Sales & Marketing

Grenoble (France)
R&D, Magnetic Materials
Processing

Russia
Crocus Nano Electronics
Manufacturing

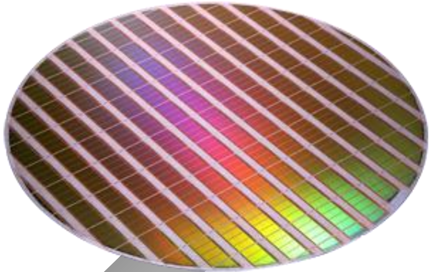
Migdal Haemek (Israel)
Tower Semiconductor
Commercial Foundry

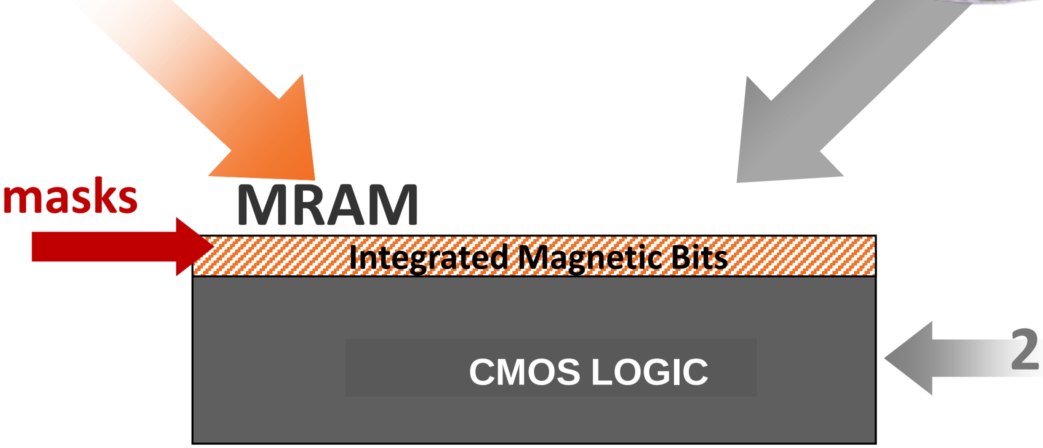
Partners:
SVTC
spintec
TOWER SEMICONDUCTOR LTD.
РОСНАНО

What is MRAM?

Disk Drive:
Magnetic Technology
(20 years of technology experience)

Semiconductor:
Speed & Logic CMOS

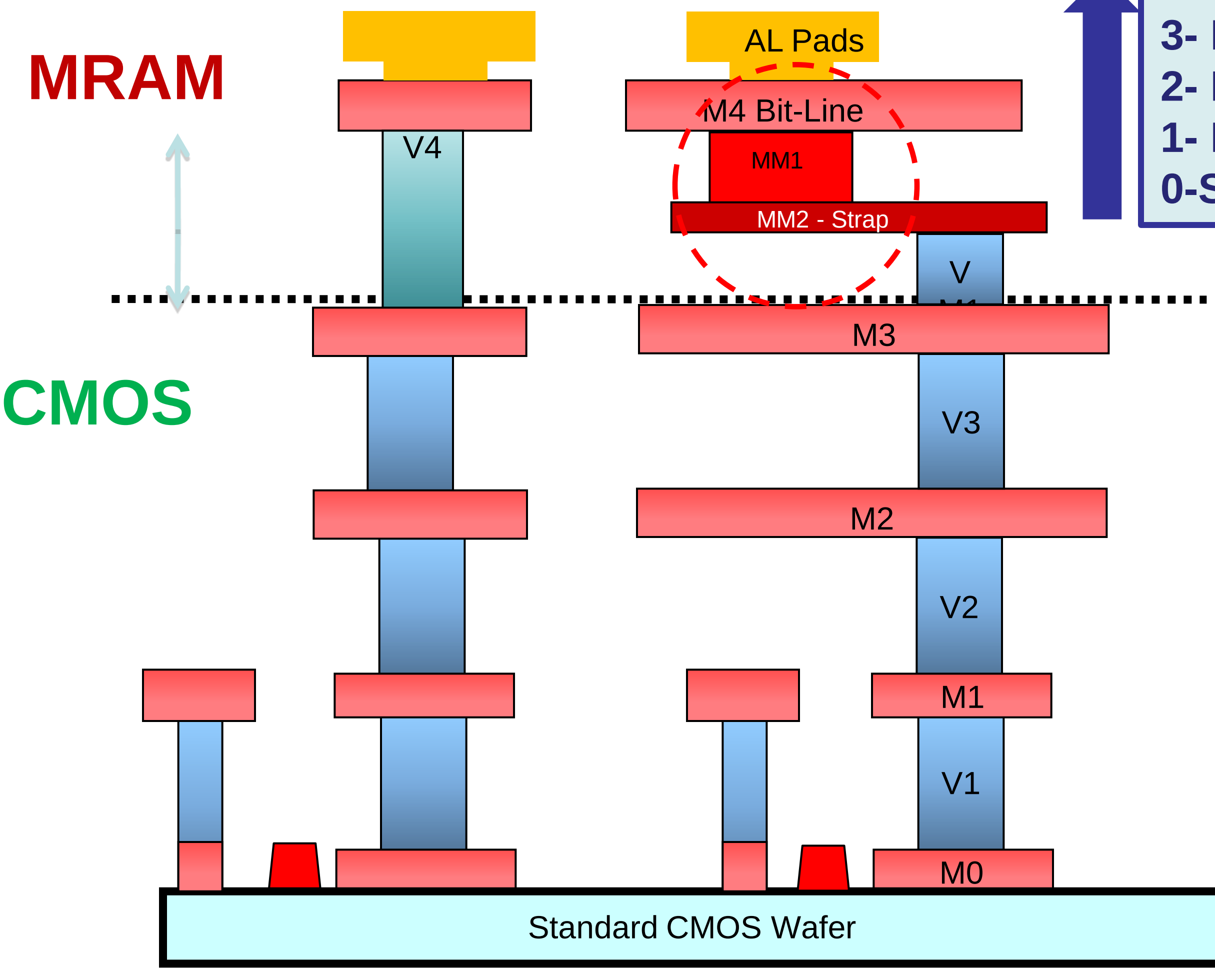




Value Add 3 masks

25-40 Mask Layers

Technology:
Process Schematic



4- Preparation final interconnect
3- Dielectric refill
2- Magnetic layers etch
1- Magnetic layers deposition
0-Surface preparation

4- Connection to MRAM
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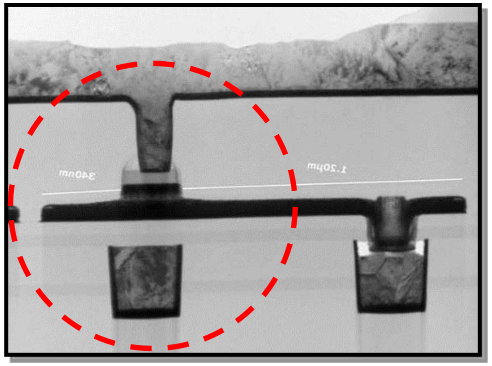
1- CMOS frontend



The search for the "universal memory"

The Universal Memory:

-Non volatile ☑

-Fast as SRAM ☑

-Dense as DRAM

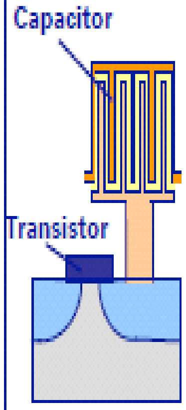
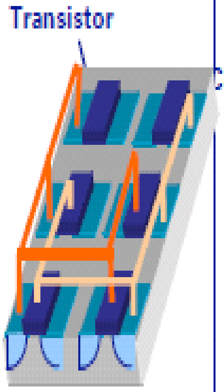
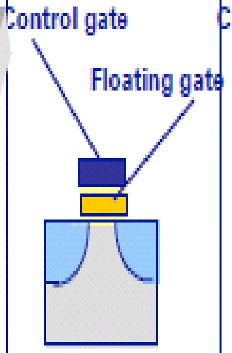
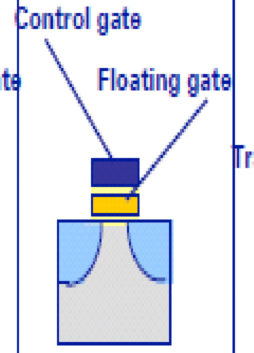
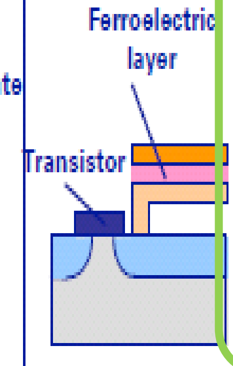
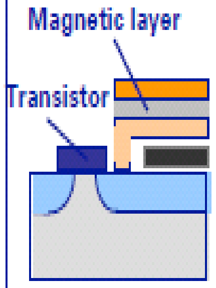
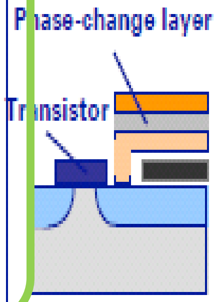
-Infinite endurance ☑

-Easy / cheap to embed into ASIC ☑

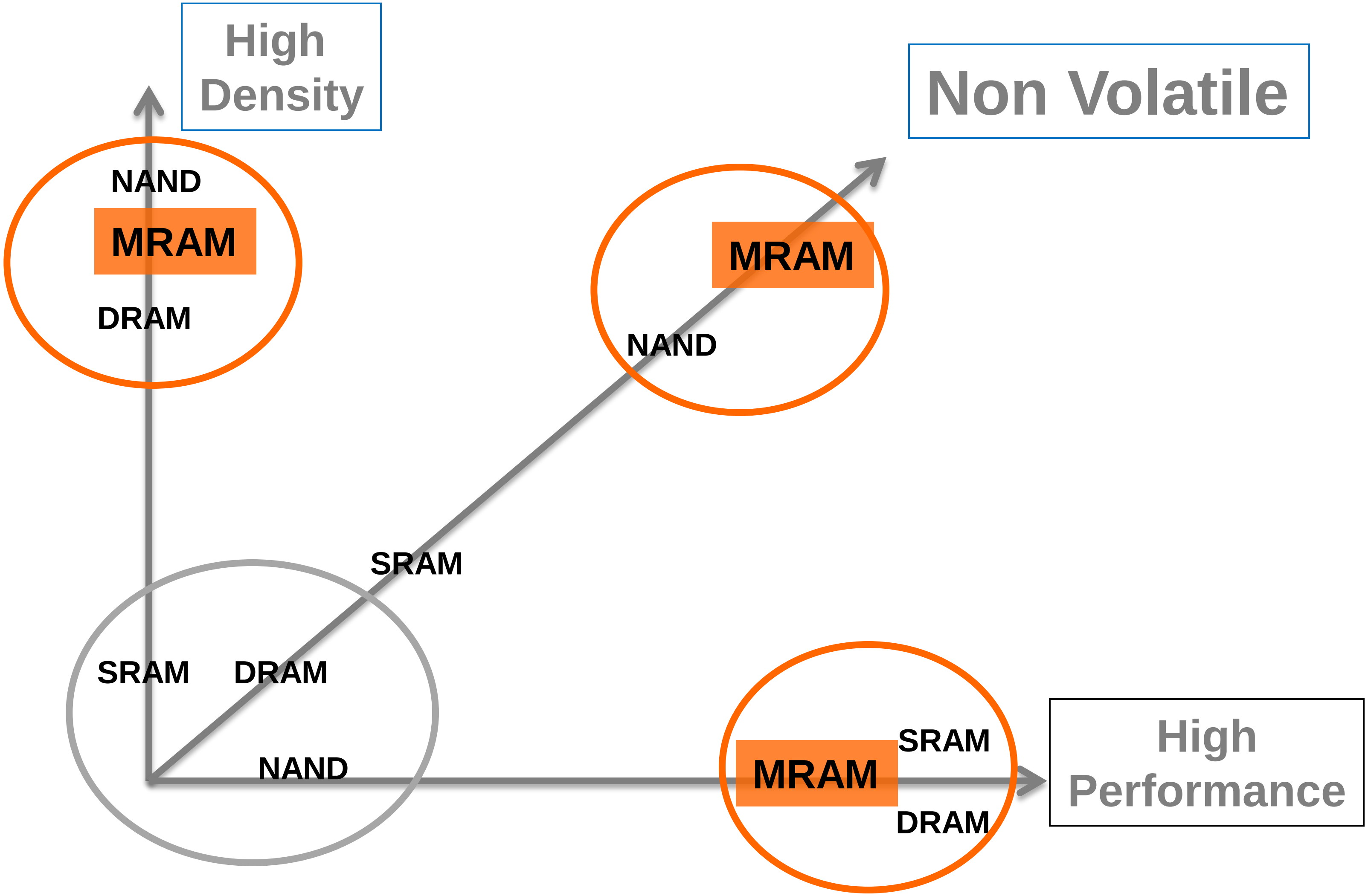
-Zero stand-by current ☑

-Fully scalable ☑

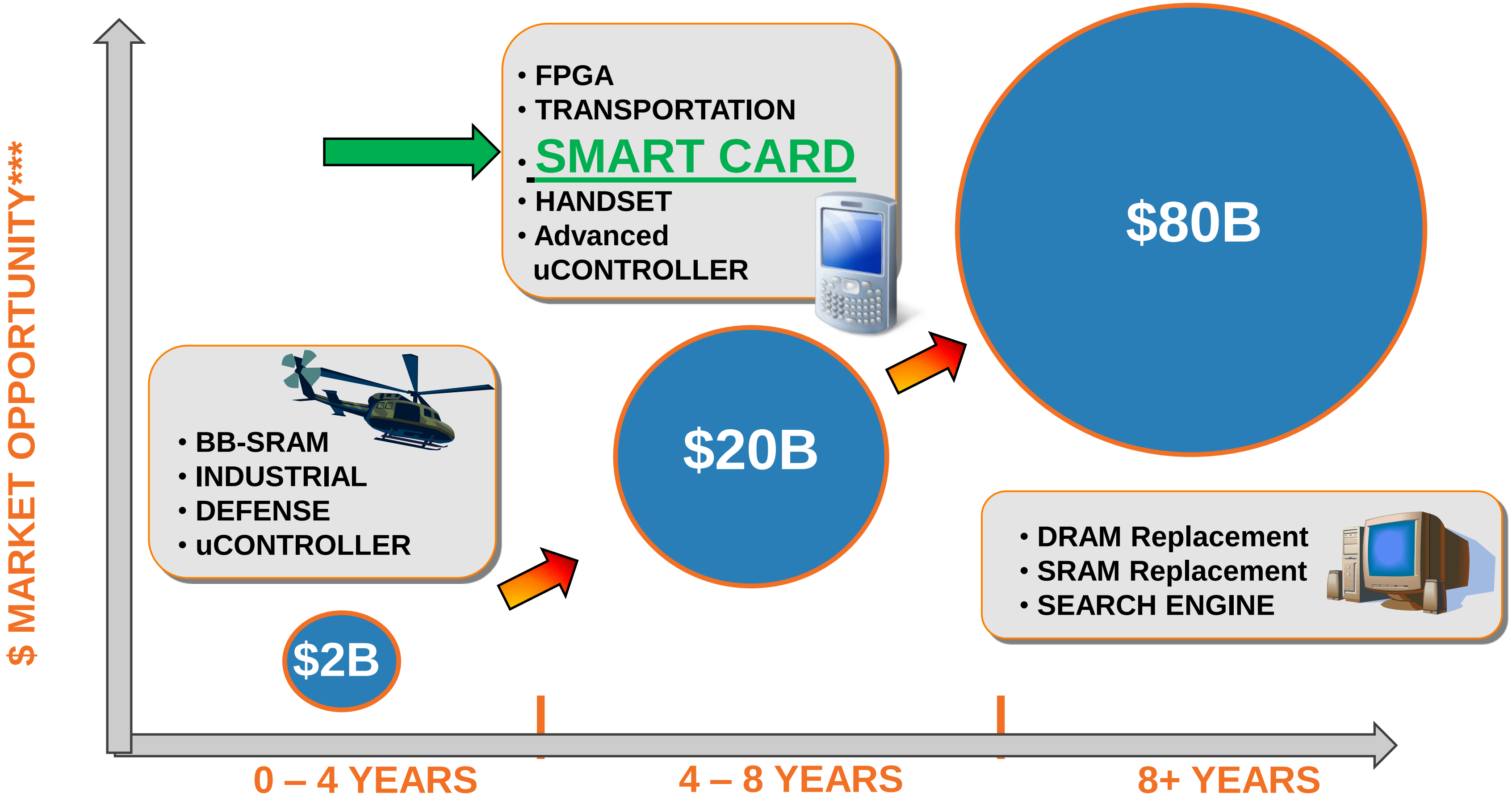
MRAM vs. other Memories

	DRAM	SRAM	NAND Flash	NOR Flash	FRAM	MRAM	PRAM
Stability (Not volatile)	NO	NO	YES	YES	YES	**YES**	YES
Current max size	4Gb	128Mb	32Gb	2Gb	16Mb	**16Mb>8Gb**	512Mb
Write speed	10ns	5ns	1000ns	1000ns	100ns	**15ns**	100ns
Read speed	10ns	5ns	1000ns	50ns	15ns	**15ns**	15ns
# of rewrites	10**16	10**16	10**3	10**4	10**10	**10**12+**	10**6
MLC	NO	NO	YES	YES	NO	**Yes**	?
Cell size	$6F^2$	$80F^2$	$4F^2$	$10F^2$	$30F^2$	**$8\text{-}25F^2$**	$10F^2$
Structure	1Tr+1C  	6Tr  	1Tr  	1Tr  	1Tr+1C  	1Tr+1C  	1Tr+1C 

the Quest…
THE Universal Memory



MRAM Field of Use



$ MARKET OPPORTUNITY***

- BB-SRAM
- INDUSTRIAL
- DEFENSE
- uCONTROLLER

$2B

- FPGA
- TRANSPORTATION
- SMART CARD
- HANDSET
- Advanced uCONTROLLER

$20B

$80B

- DRAM Replacement
- SRAM Replacement
- SEARCH ENGINE

0 – 4 YEARS

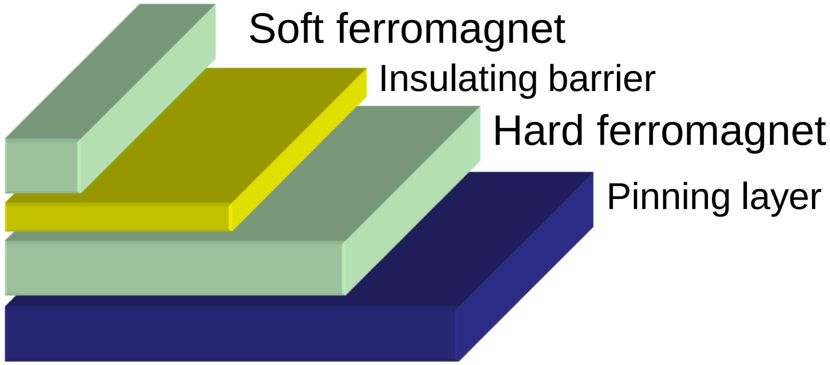
4 – 8 YEARS

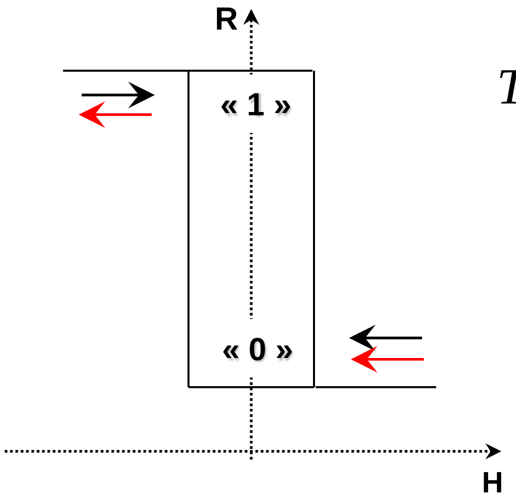
8+ YEARS

*** Source: industry data quest

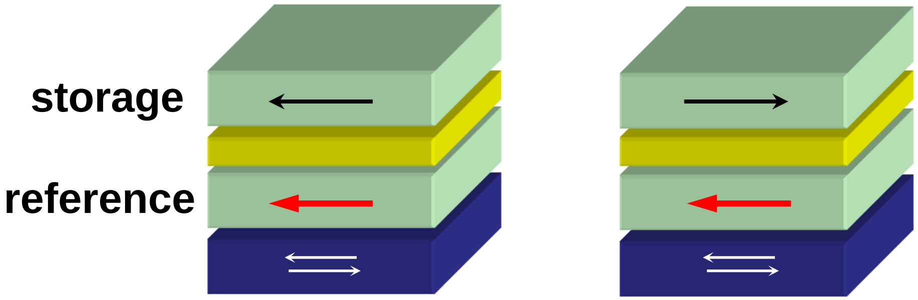
MTJ: the heart of *MRAM bit cell*

MTJ structure





$$TMR = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}}$$

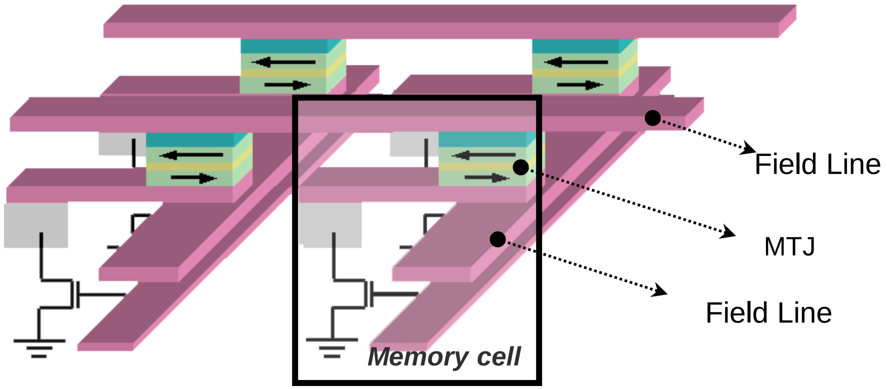


Parallel moments

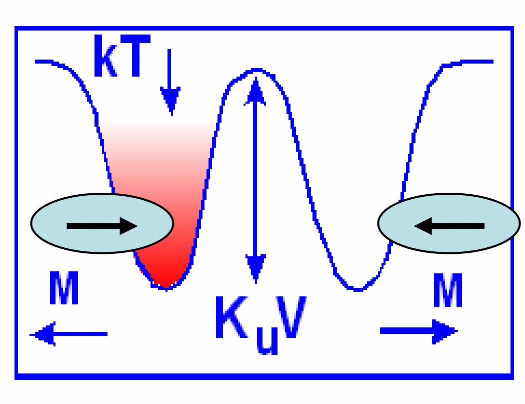
low R state

Anti-parallel moments

high R state



Scaling : the stability issue



Switching rate

$$\tau = \tau_0 e^{\frac{KV}{k_B T}}$$

Stored magnetic energy

Thermal energy

$(\tau_0 = 10^{-9}s)$

Switching probability

$$P_{\pm} = 1 - e^{-\frac{t}{\tau_{\pm}}}$$

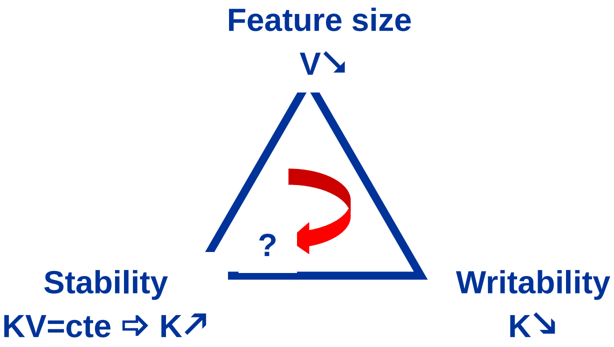
$\boxed{\text{10 years retention} \rightarrow KV/k_BT>60}$

As V goes down tendency to self-demagnetize gets worst

→ Superparamagnetic limit
(also observed in HDDs)

Only solution is to increase barrier height

→ The « storage trilemna »



Feature size
V↘

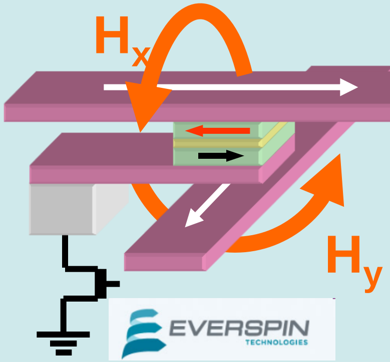
?

Stability
KV=cte ⇨ K↗

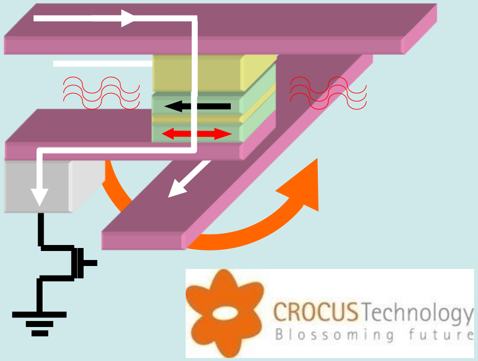
Writability
K↘

There are many MRAMs !

Field-driven

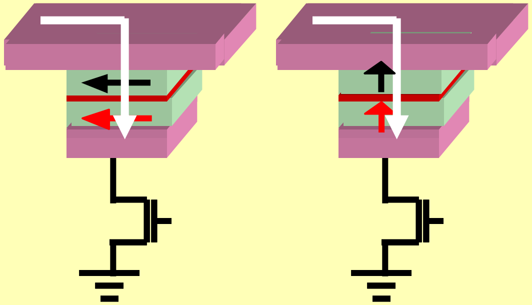


Thermally Assisted (TAS)

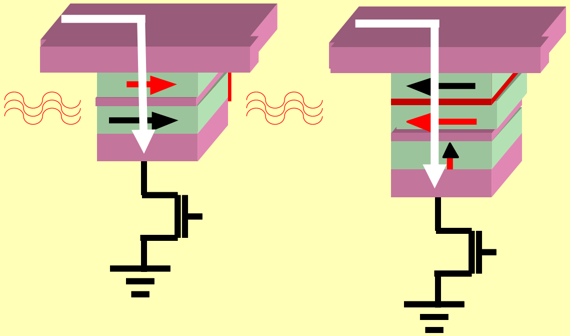


STT (SPRAM)

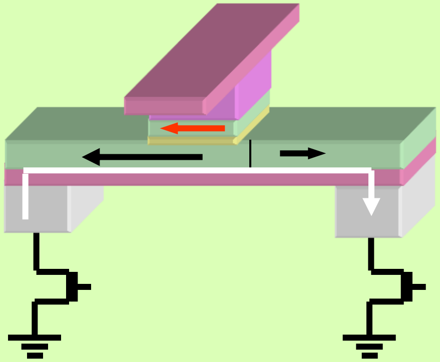
Planar Perpendicular



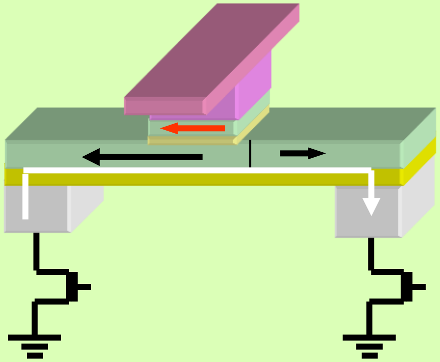
STT-TAS Precessional



DW motion



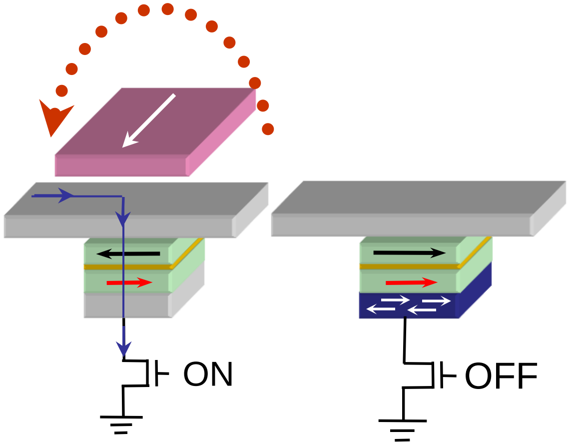
STT Domain Wall motion



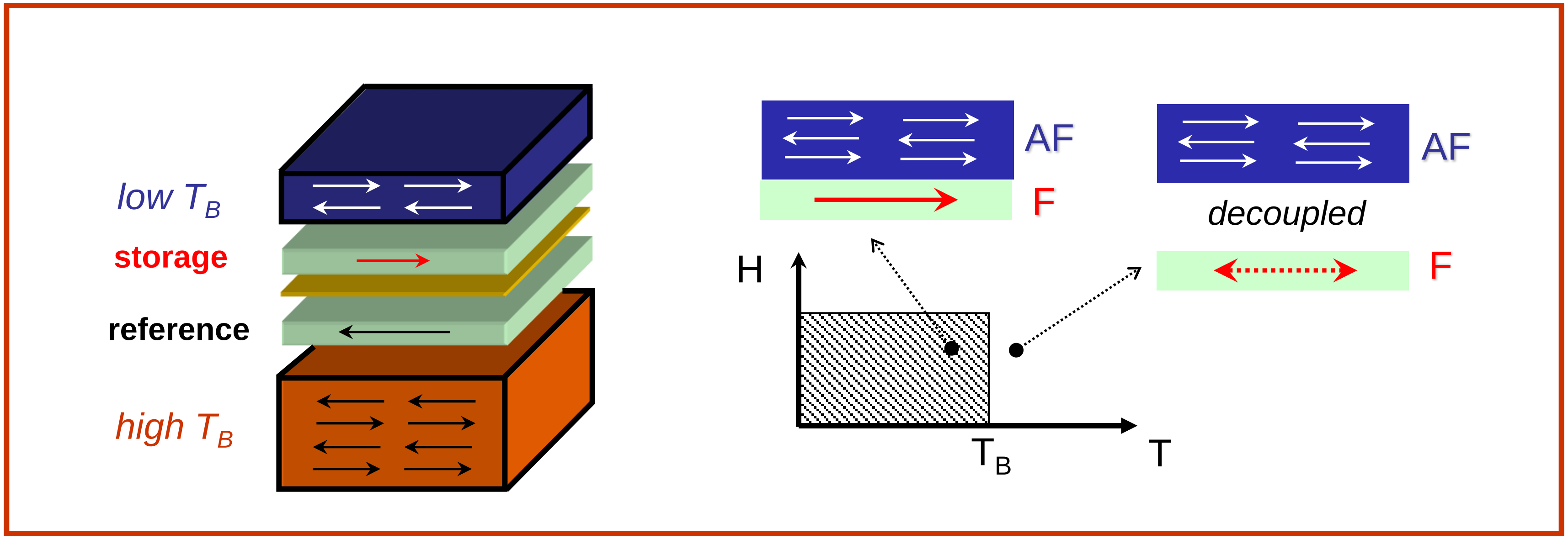
TAS-MRAM
Thermally assisted writing

❖ Use of an additional AF material to “lock” the stored data: storage layer is an F/AF **exchange biased bilayer**: **high stability @ small feature size**

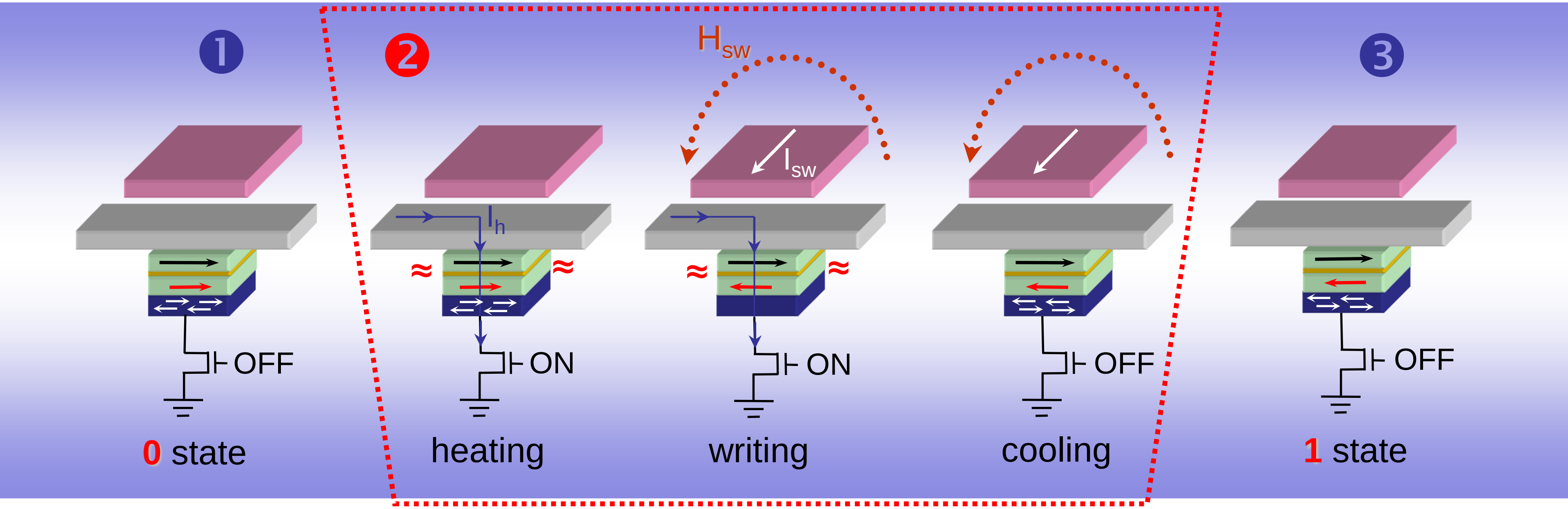
❖ The data can be “unlocked” by locally heating the memory cell - use current flowing through the junction to **heat the storage layer** above its blocking temperature: **perfect selectivity**

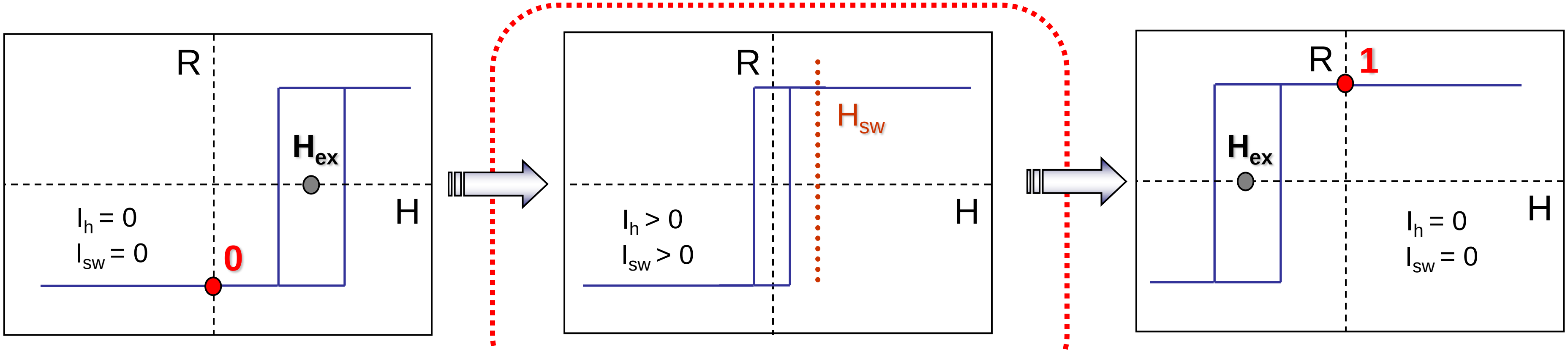


❖ Switch the storage layer by a **single magnetic field**



TAS writing





T = room temperature

T > writing temperature

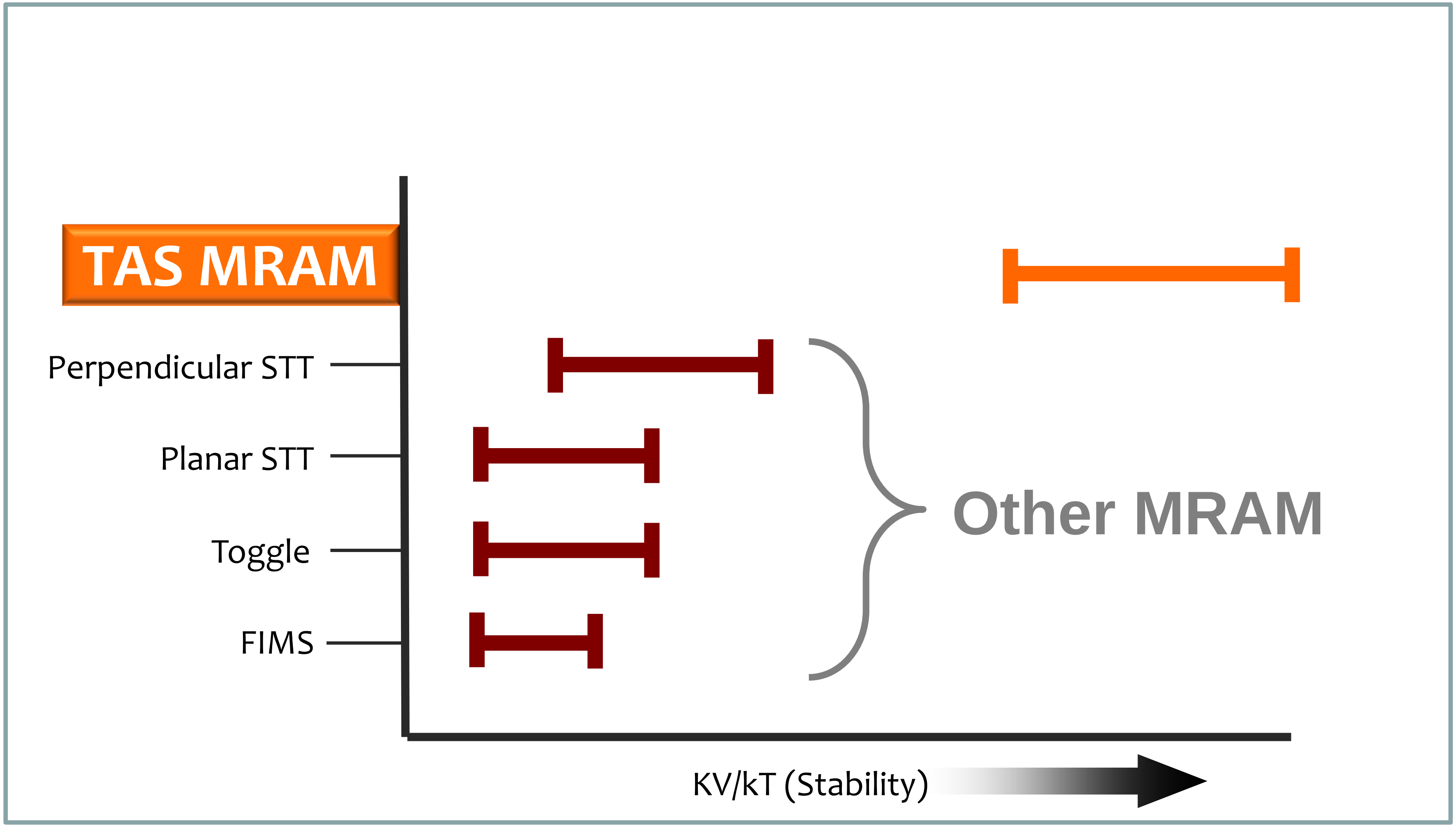
T = room temperature

Step 1: Heat cell by flowing current through transistor

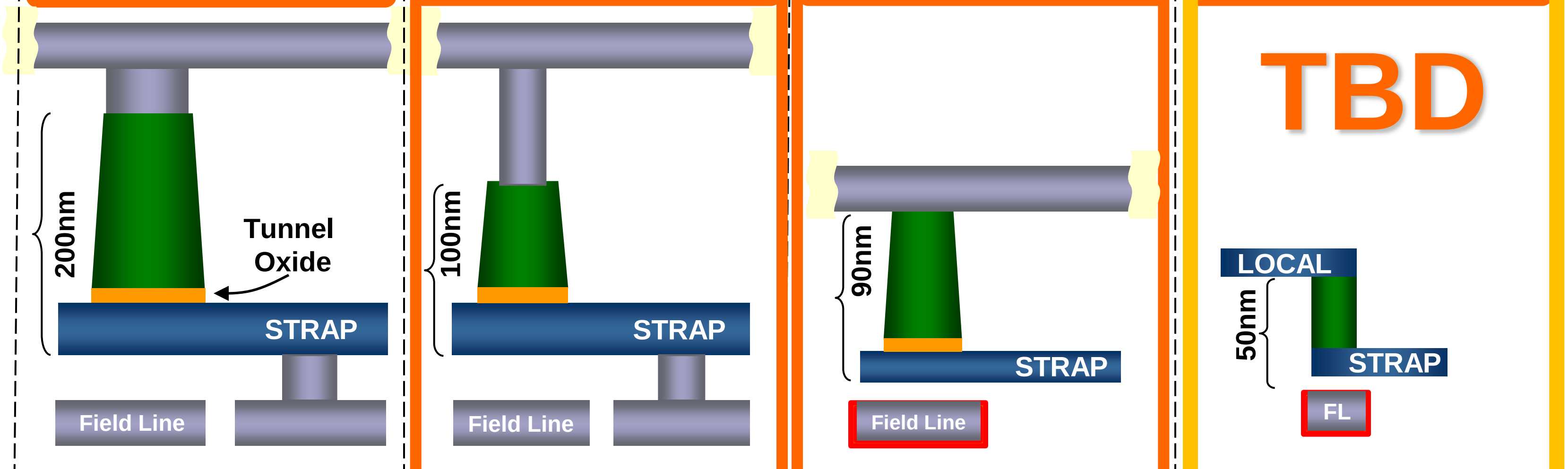
Step 2: Switch magnetization by a magnetic field pulse

Step 3: Cool under magnetic field

From MRAM to MLU: Stability



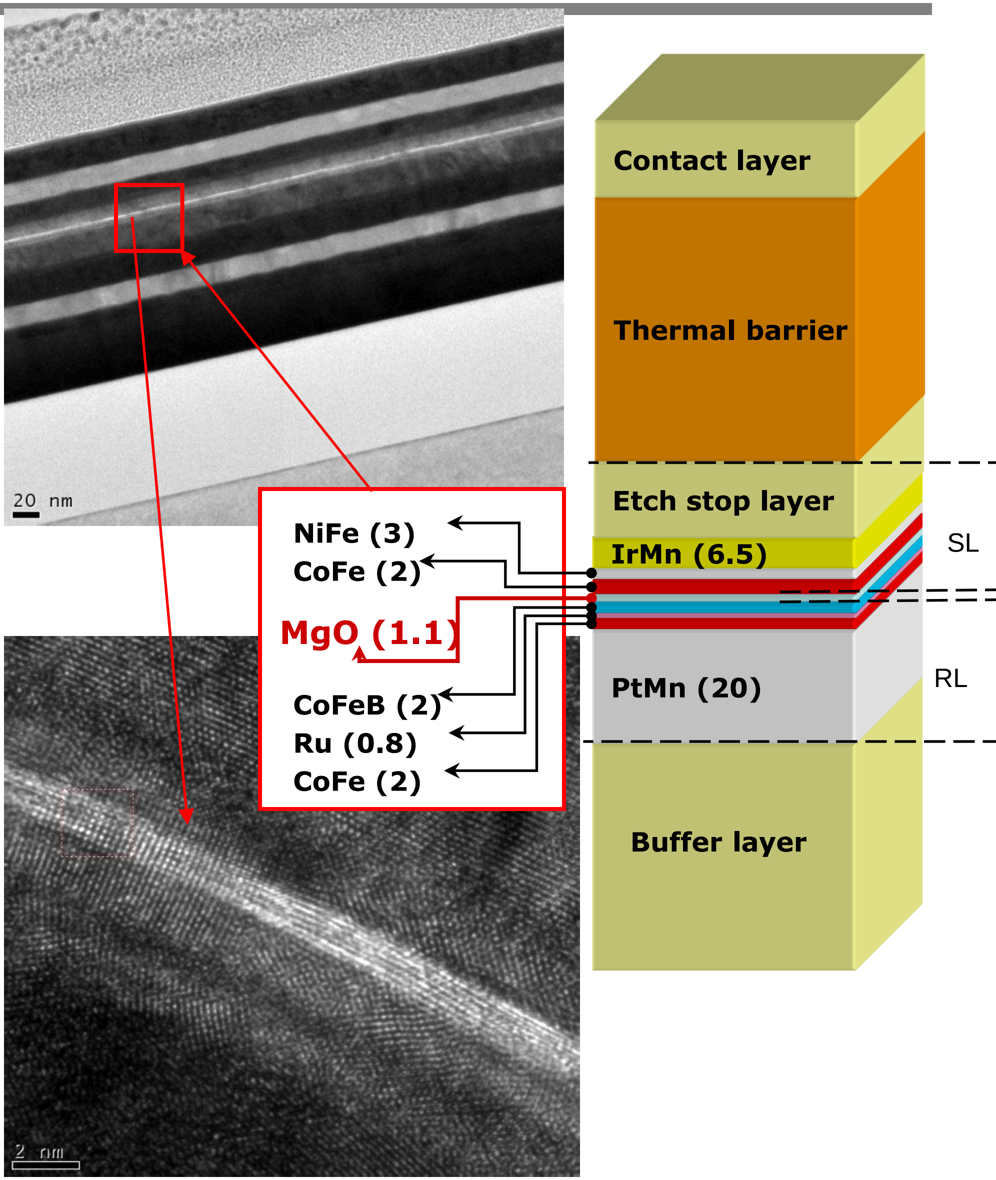
Technology:
Process Roadmap



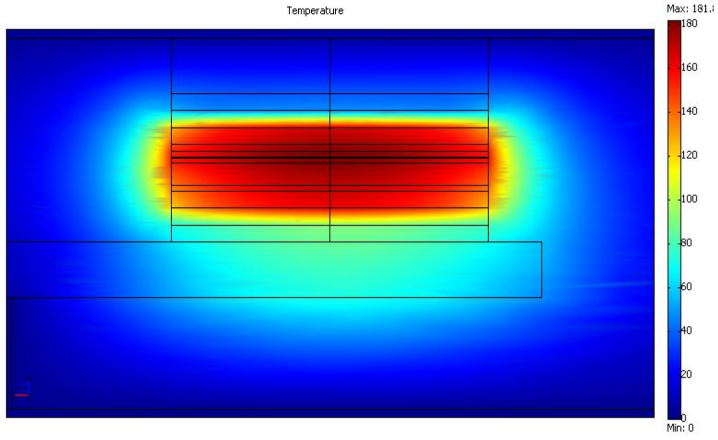
	GENERATION 1	Tower GENERATION 2	IBM/CNE GENERATION 3	GENERATION 4
CD	200nm	120nm	90nm/65nm/45nm	28nm/15nm
IField	30mA	20mA	2mA	500uA
ITAS	2A	500uA	100uA	25uA
Arch	Strap	Strap	Thin Strap	Thin strap
Masks	+ 4 Masks	+ 4 Masks	+ 2 Masks	+ 2 Mask

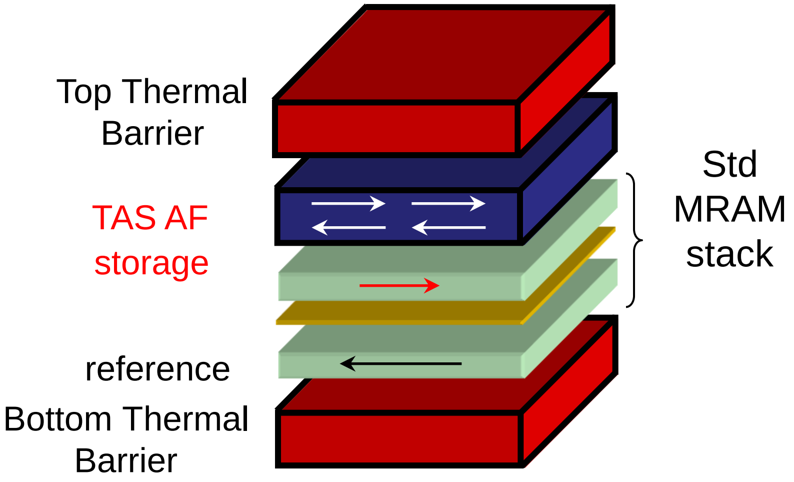
Technology:
Magnetic materials

Timaris sputtering tool
from SINGULUS
200mm wafers
Installed at Minatec, Grenoble



Technology:
Thermal Management




Top Thermal Barrier

TAS AF storage

reference

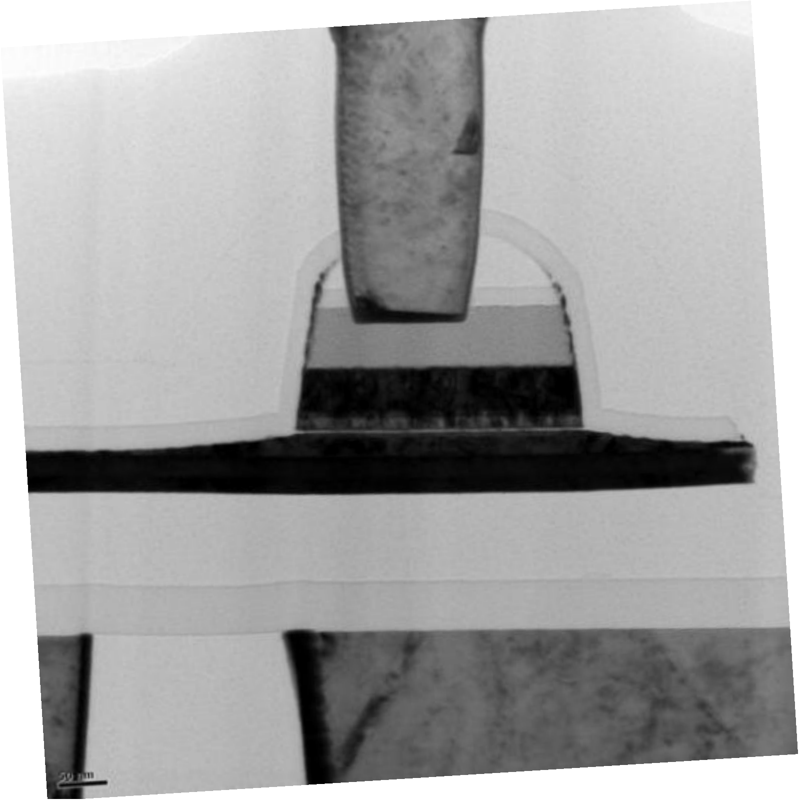
Bottom Thermal Barrier

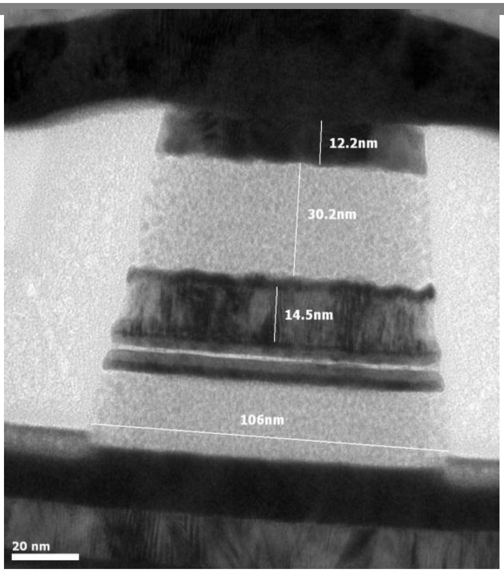
Std MRAM stack

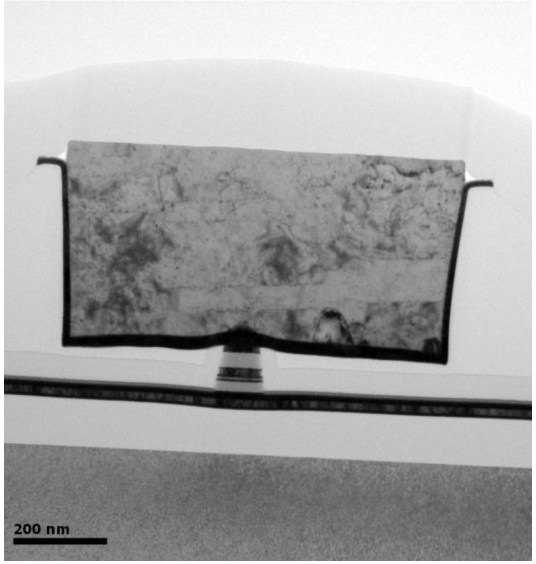
Compared to Standard MRAM, stack changes are :

- Add anti-ferromagnetic layer
- Add thermal barriers
  - Concentrate heat
  - Control temperature rise
  - Reduce heating power

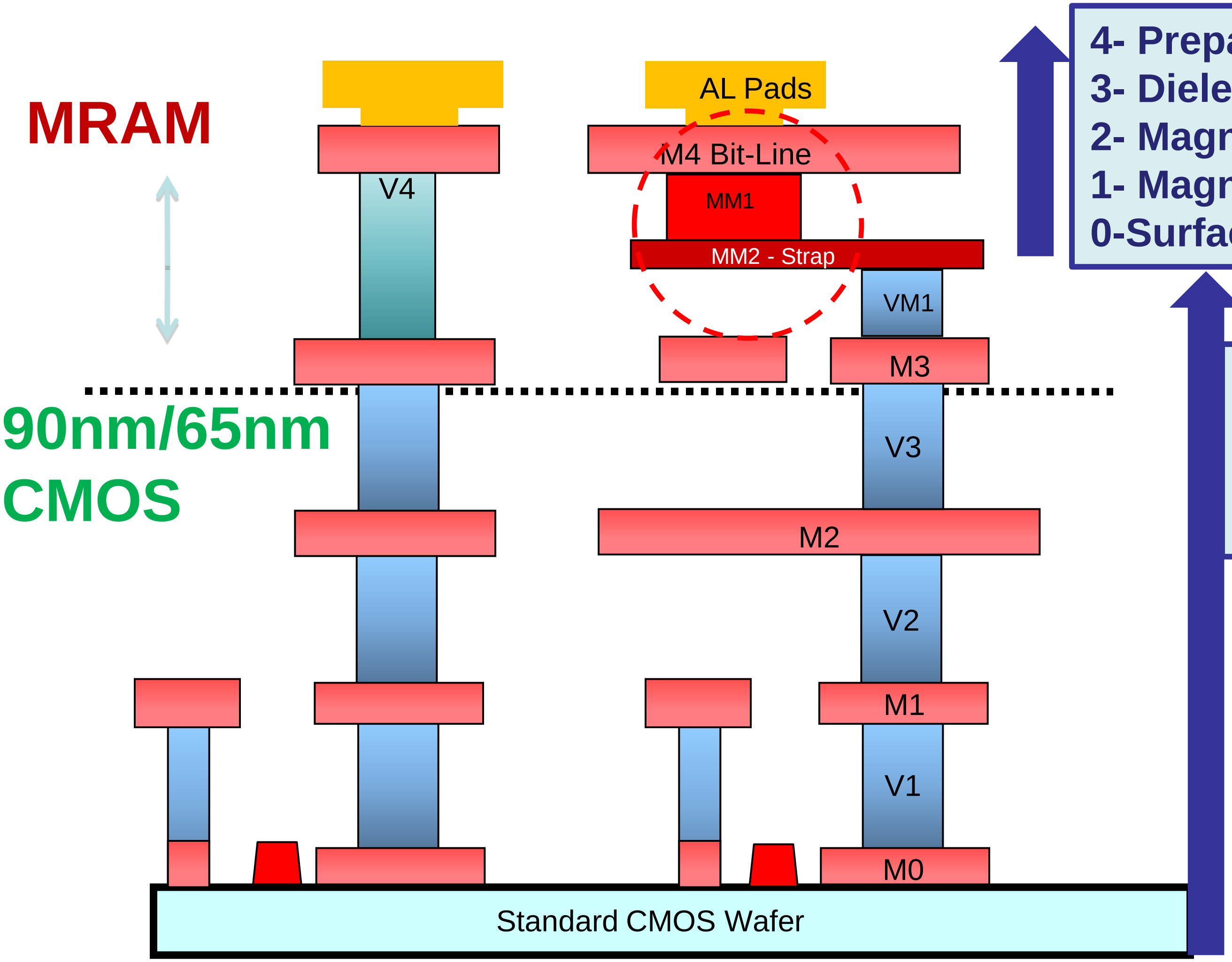
Gen2 vs. Gen3







Technology:
Process Schematic



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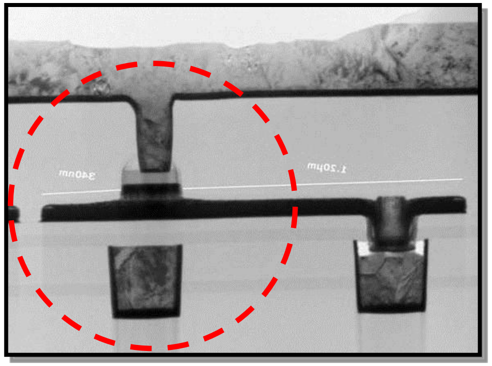
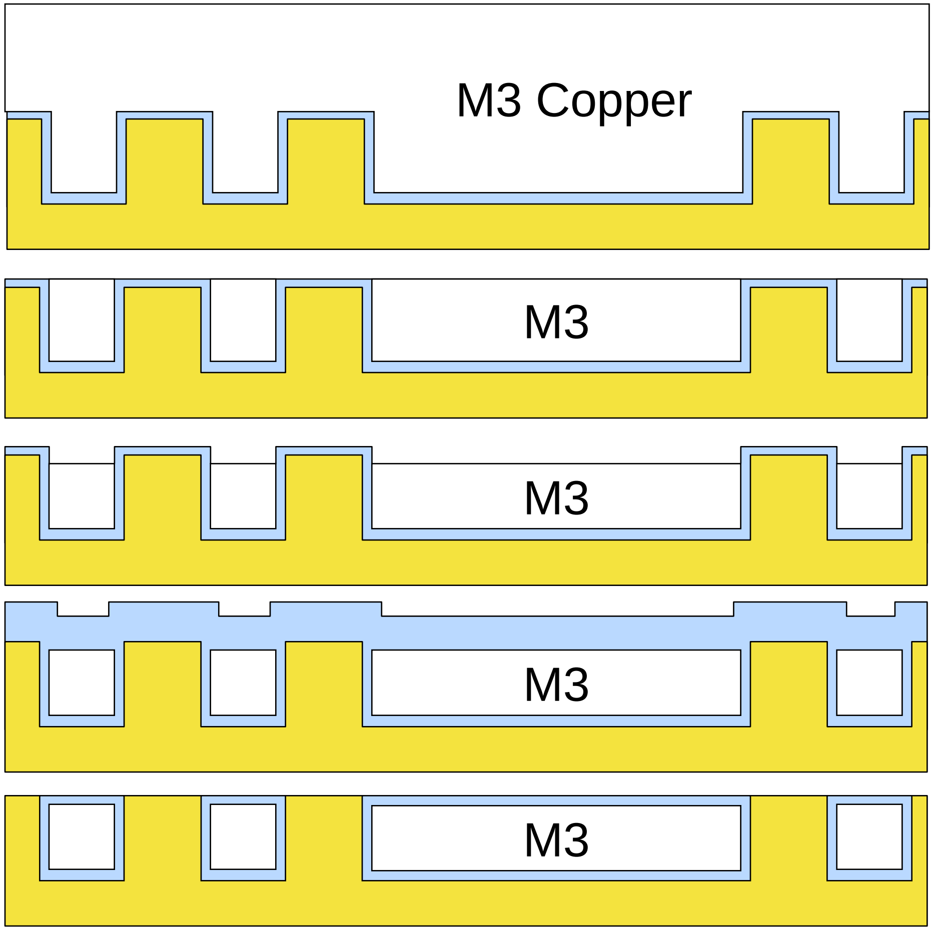
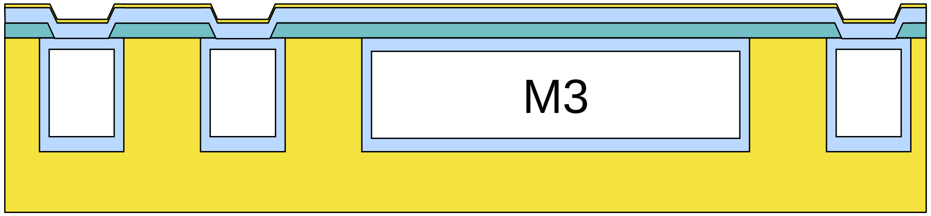


Technology:
GEN 3 PROCESS FLOW

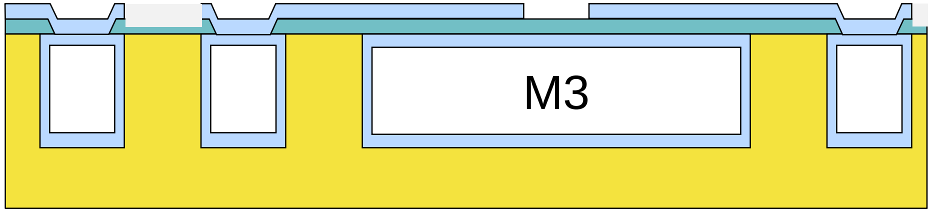


- Receive CMOS wafer from Foundry after dielectric deposition
- Metal trench Litho and etch
- Cladding deposition (PVD). Co
- Cu Damanscene (PVD) Std Cu seed
- Top Cladding Deposition (PVD) Ta
- CMP Top Cladding metal

GEN 3 PROCESS FLOW

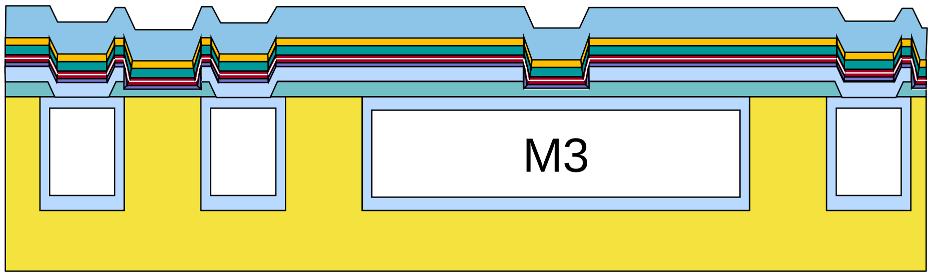


- Deposit Dielectric and open Via
- Deposit Strap Metal (PVD). Ta

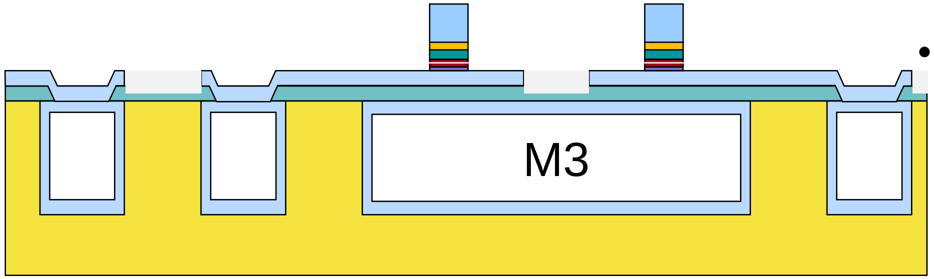


- Pattern Strap Metal
- Etch Strap Metal

GEN 3 PROCESS FLOW

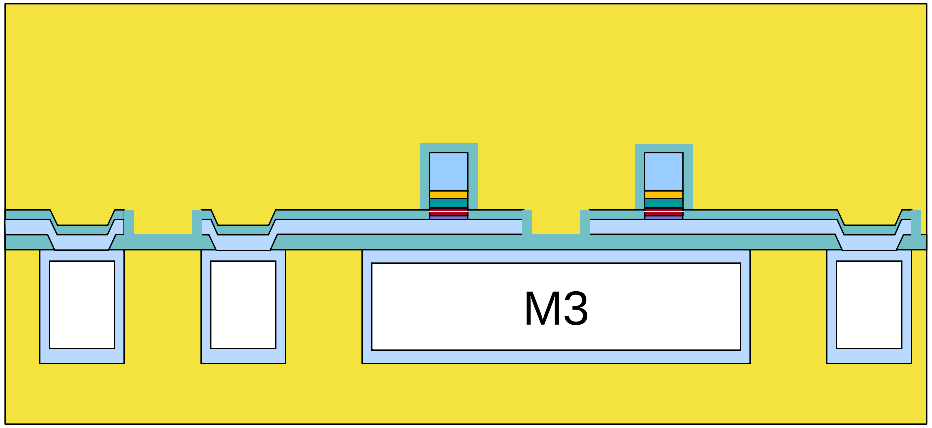


- **Deposit Magnetic Stack (PVD)**
  -Total of 10 -12 thin layers. 7 to 8 different materials : Ta, Ru, FeMn, CoFe, CoFeB, Mgo, NiFe
  - Precise thickness and film morphology control

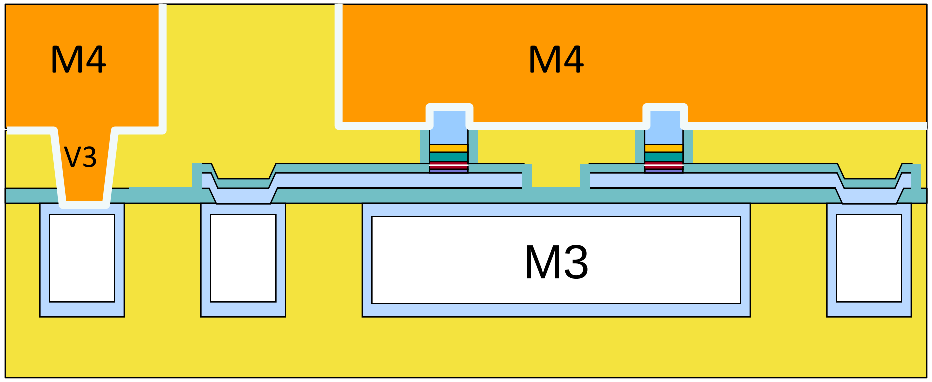


- **Magnetic Stack Etch**
  - Precise side wall control
  - No redeposition and short
  - Post shape control
  - Magnetic film affected by Cl and F etch

GEN 3 PROCESS FLOW

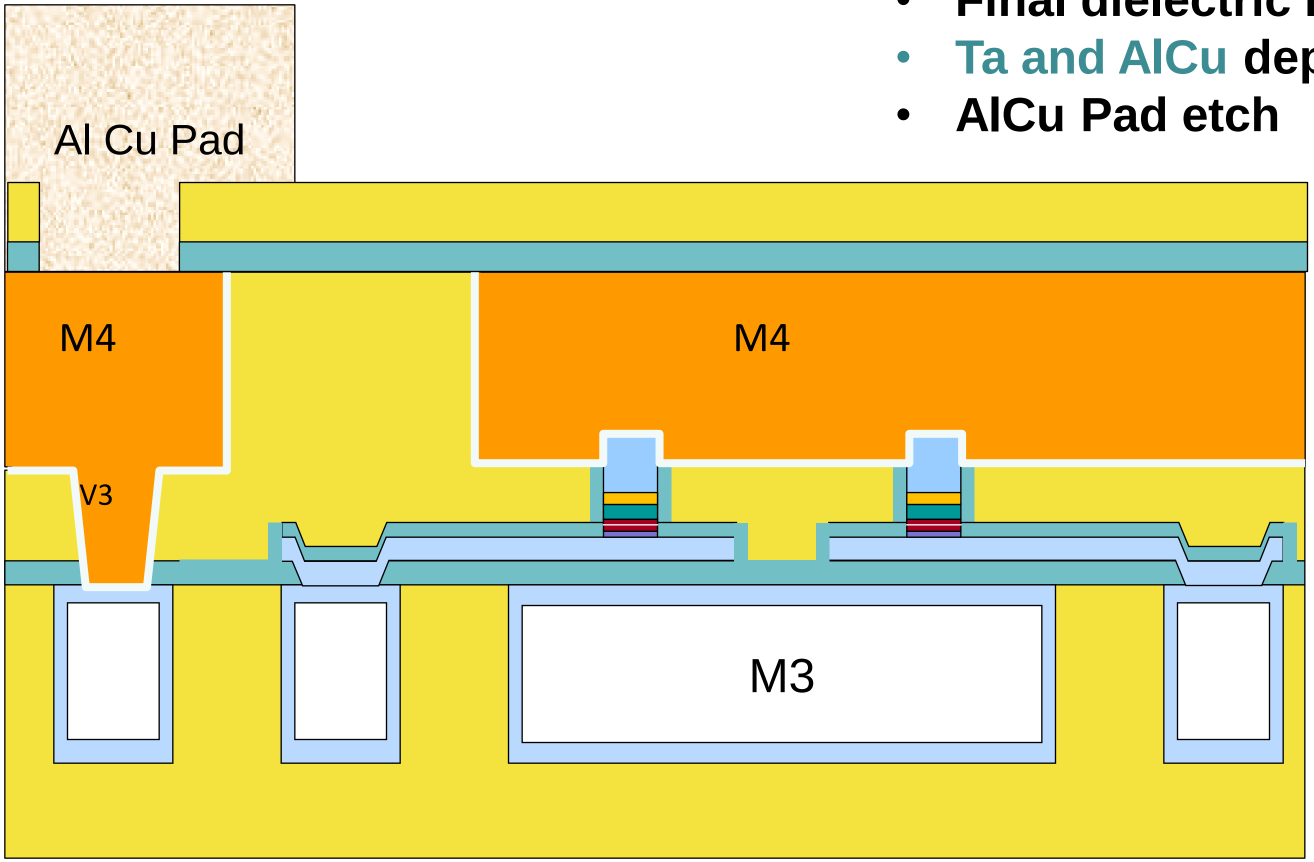


- **Dielectric Deposition**



- **Via First Cu Dual Damanscene process (PVD) Ta, TaN, Cu seed**

GEN 3 PROCESS FLOW



- **Final dielectric layer deposition**
- **Ta and AlCu deposition (PVD)**
- **AlCu Pad etch**

From the Lab to the Fab :
The challenges for functional products

Functional device over 10 years and 10^{12} write cycles :

Yield for Read Head production :

1 device = 1 MTJ → 40% bit yield on a wafer is enough to make profits.

For one functional one 1Mb MRAM, bit yield within this memory has to be >99,9999%

Objective of Reliability + Yield :

→ Errors rate <10^{-6} over 10 years and 10^{12} write cycles

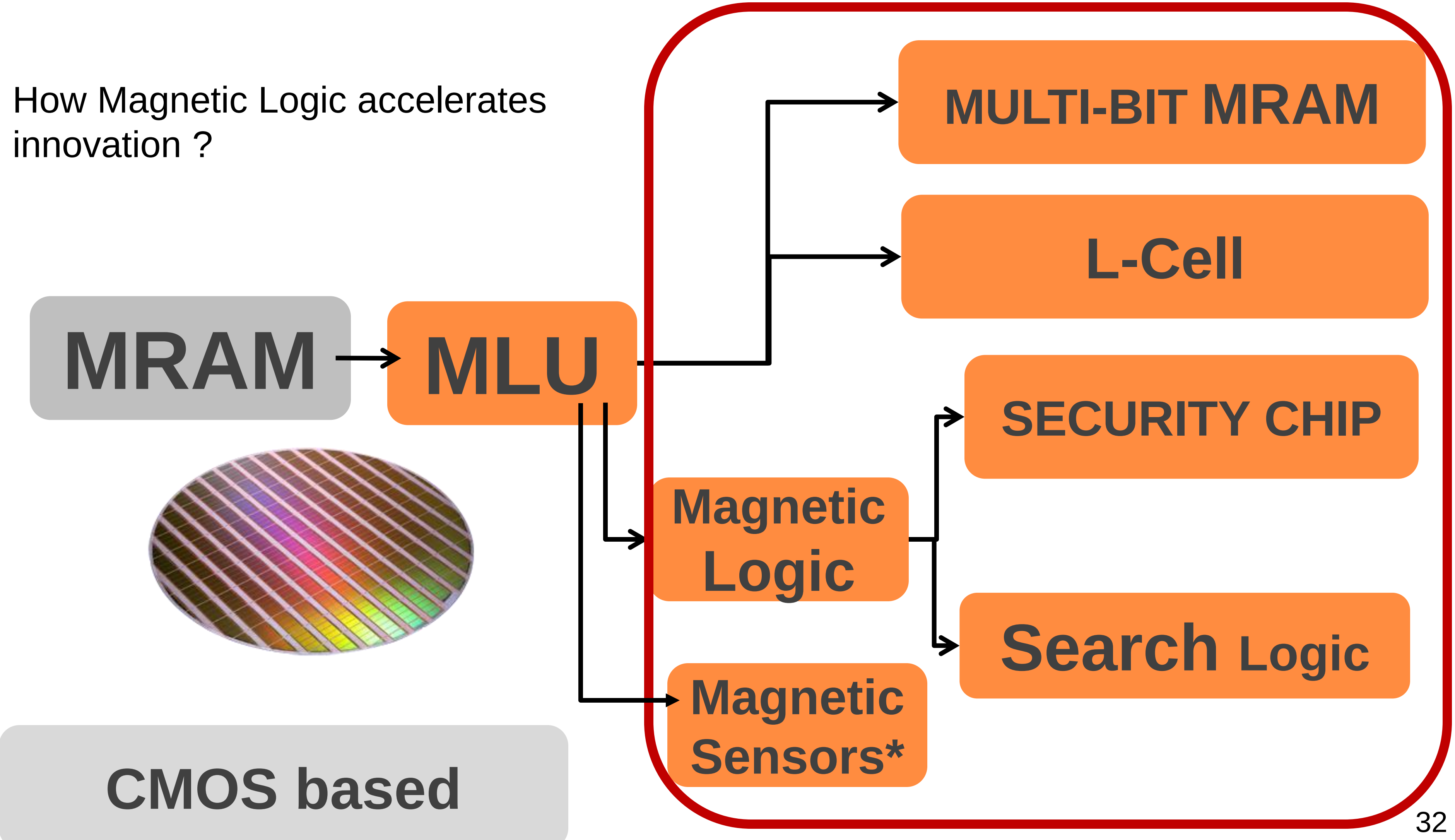
From MRAM to MLU

Magnetic Unit Logic

From MRAM to MLU

Magnetic Unit Logic

How Magnetic Logic accelerates innovation ?



MRAM

MLU

MULTI-BIT MRAM

L-Cell

SECURITY CHIP

Magnetic Logic

Search Logic

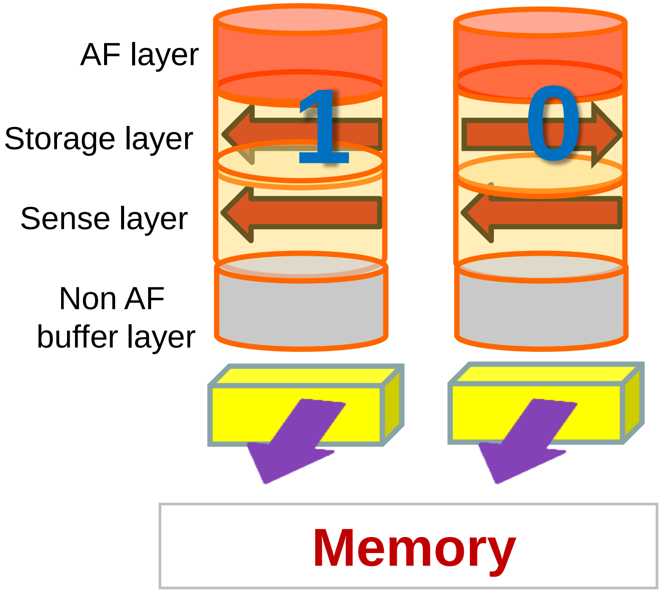
Magnetic Sensors*

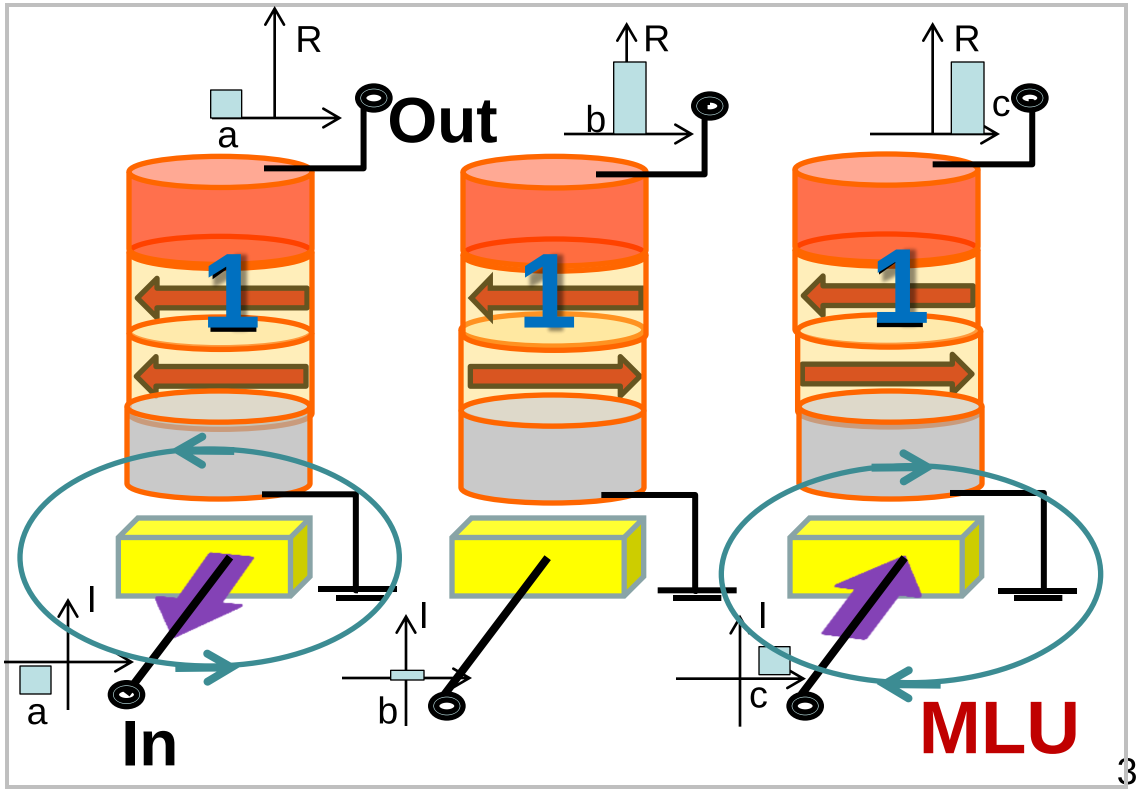
CMOS based

* No CMOS required

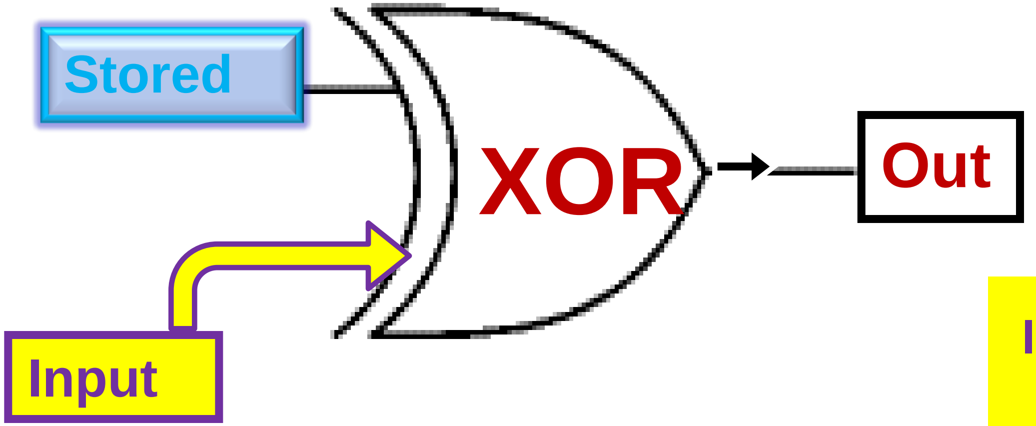
MRAM to MLU

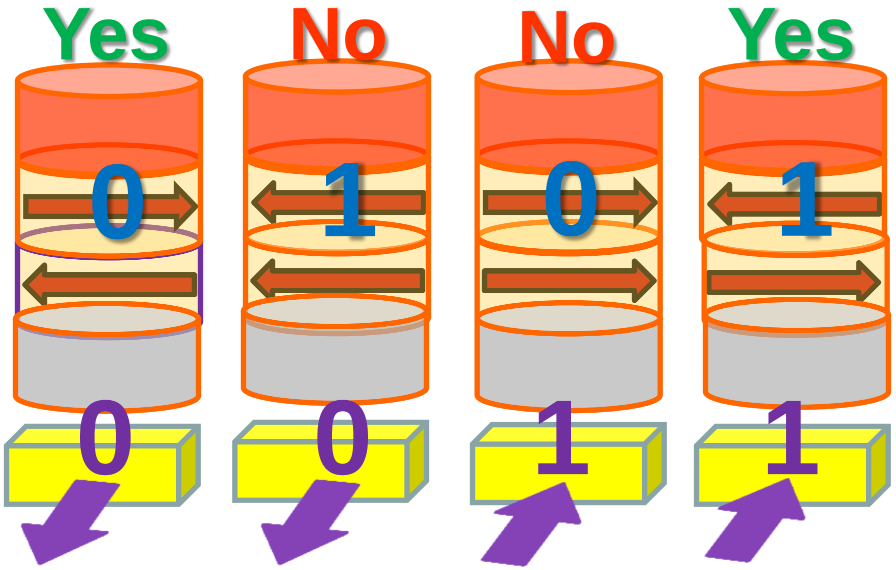
- **MRAM:** 2 states: Parallel “1”, or Antiparallel: “0”
- **Thermally Assisted Switching** (TAS): Pin storage layer
- **Self reference cell**: Reference layer becomes as sense layer for the field line
- **Magnetic Logic Unit** (MLU): 3 terminal device





Match-in-Place™

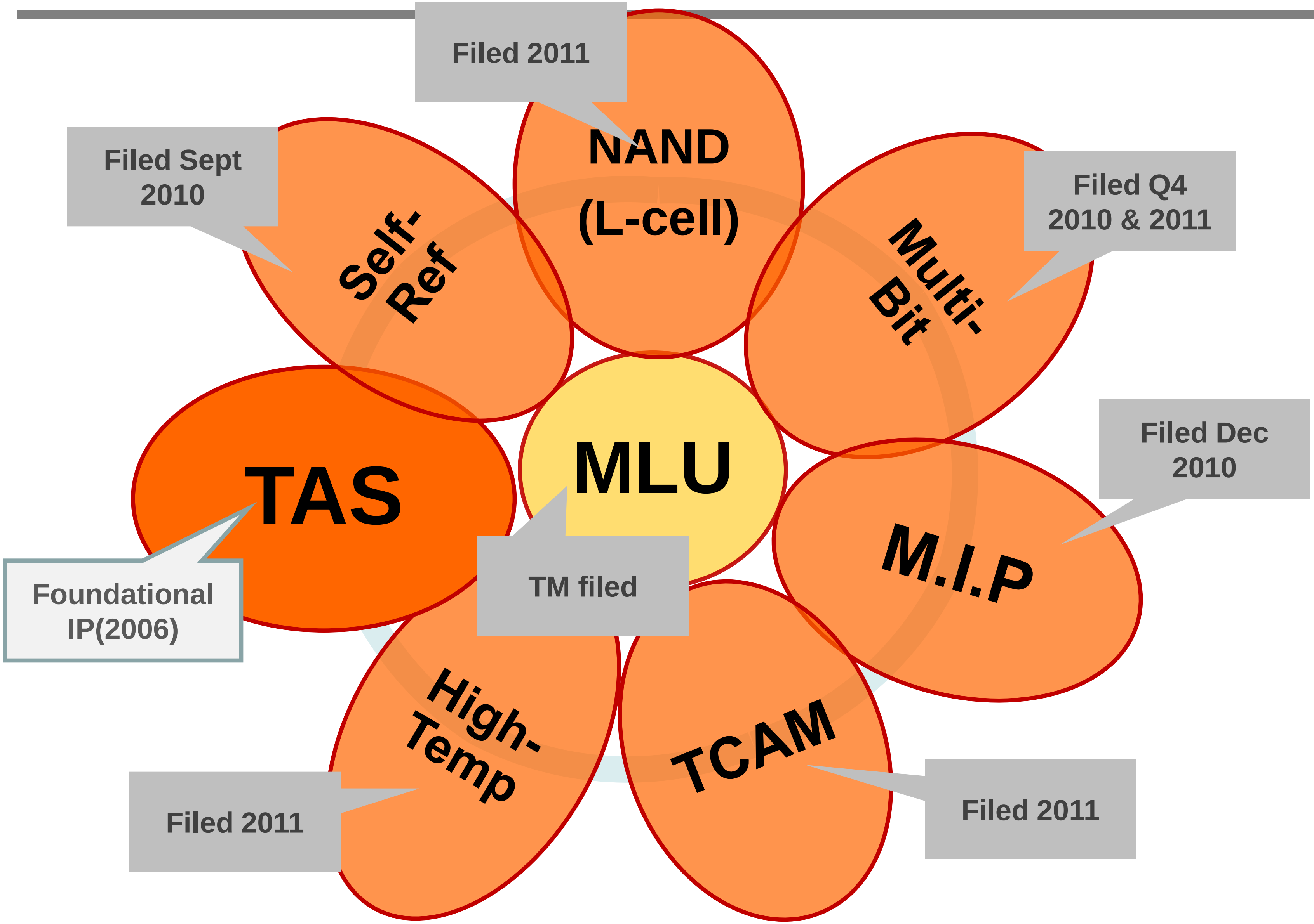




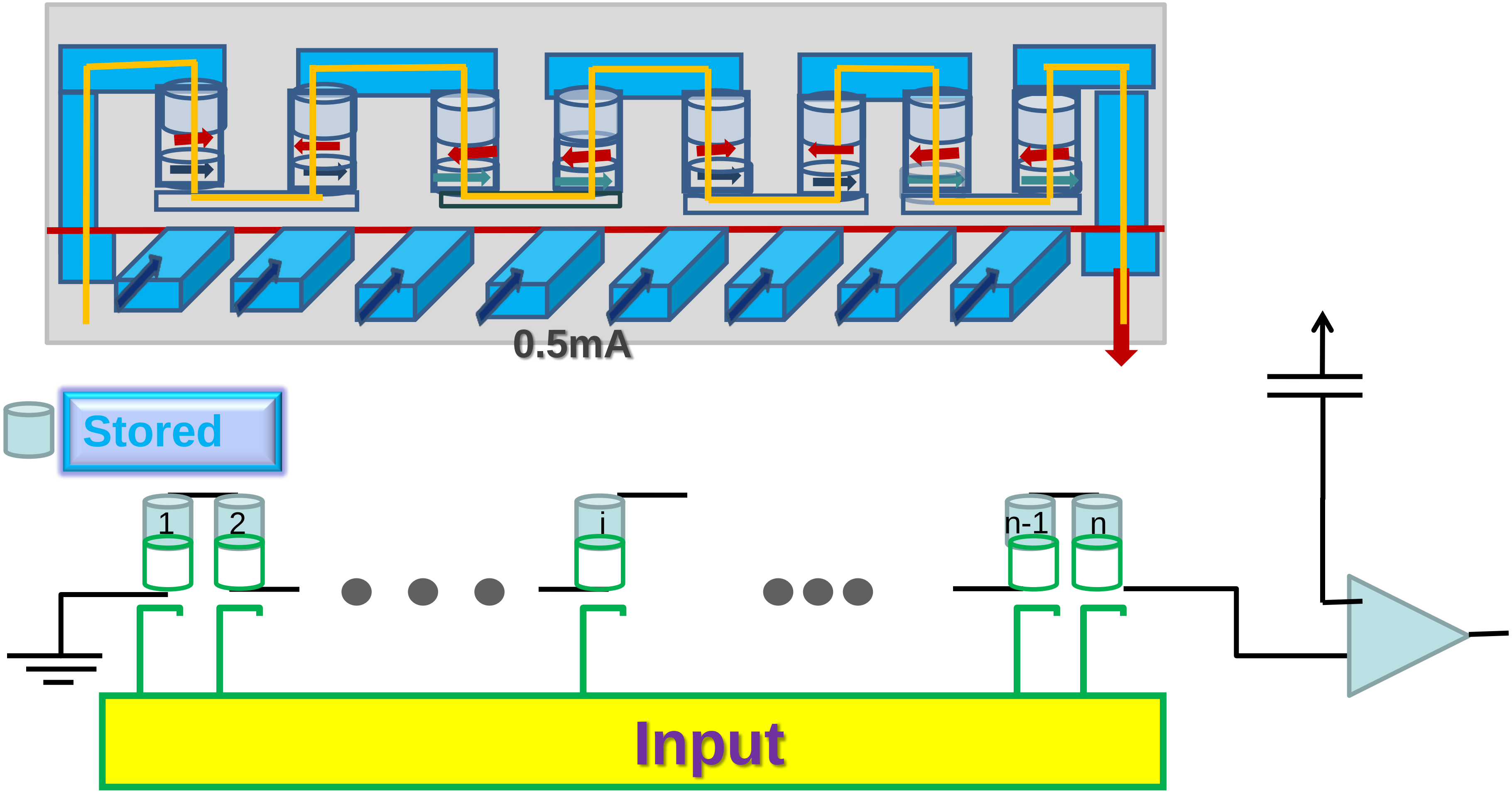
Input	Stored	Match
0	0	Yes
0	1	No
1	0	No
1	1	Yes

Accelerate innovation

From MRAM to MLU

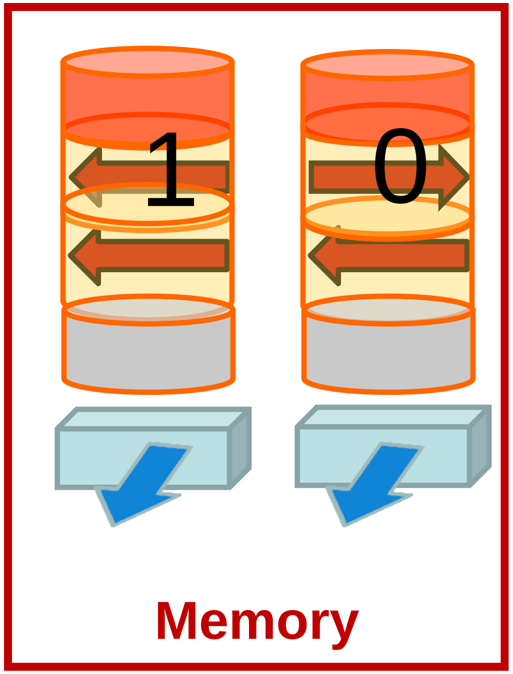


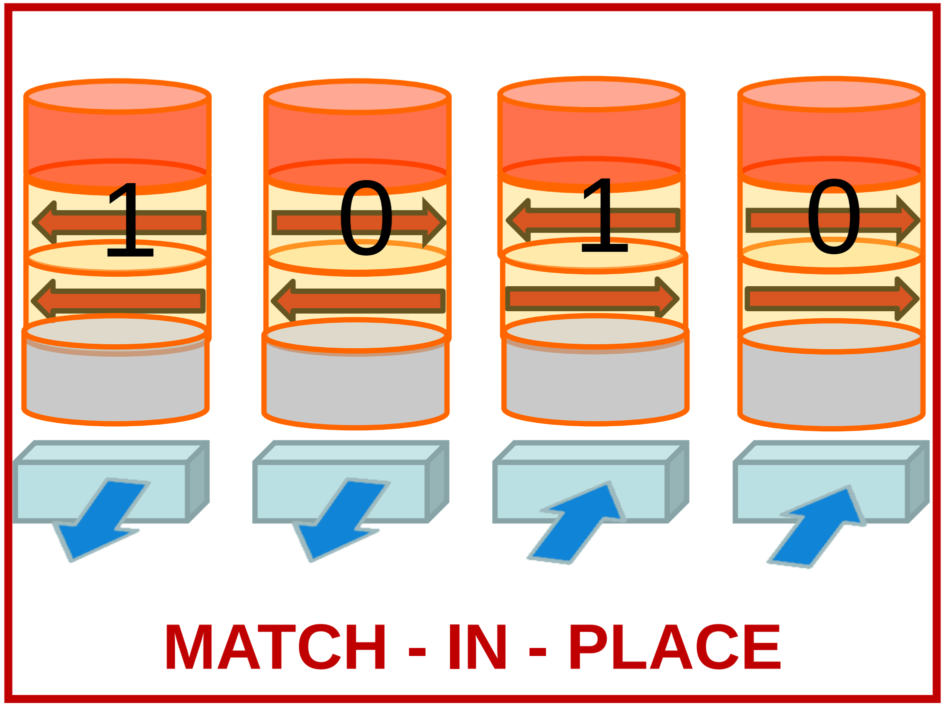
Dense L-cell



Match in Place

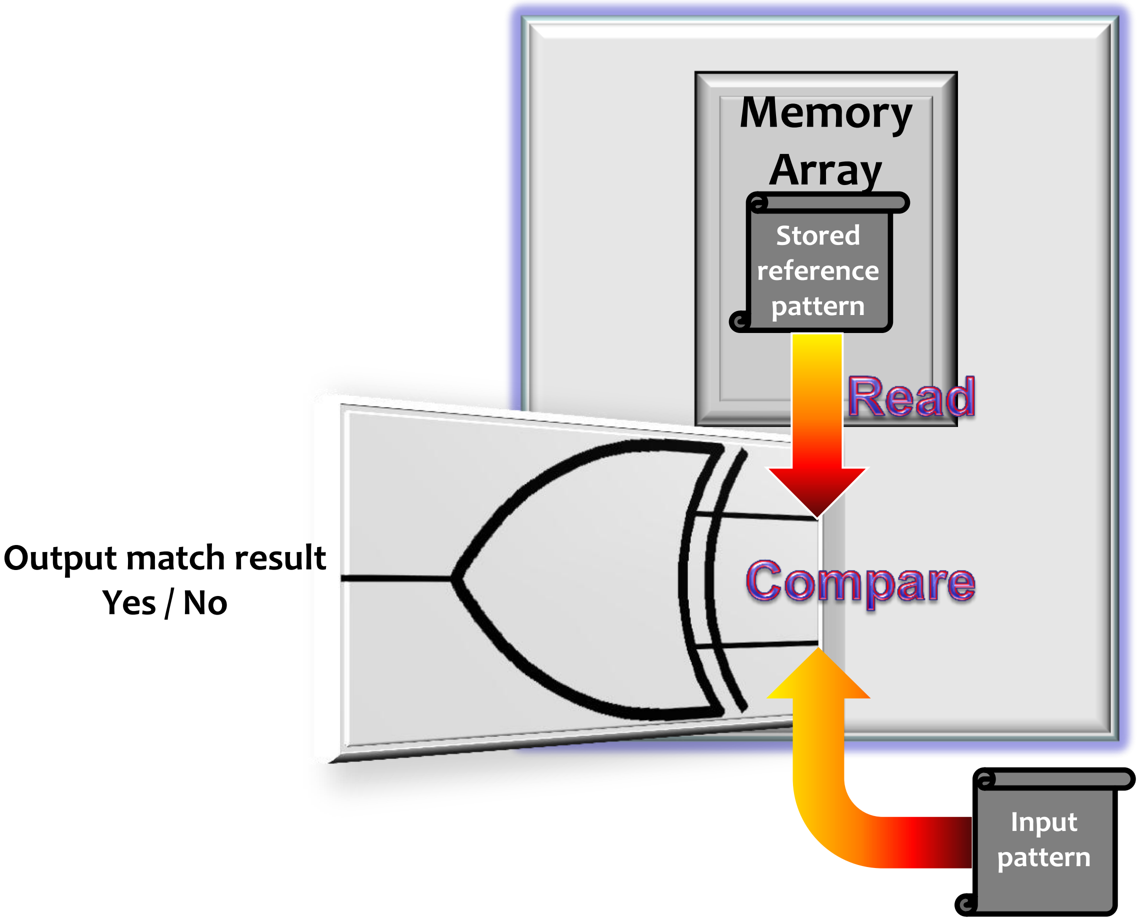
- Fully leverage TAS and self reference
- Use sensing layer for matching purpose.
  - Field lines carry the input key
- Stored key is blocked by the top AF



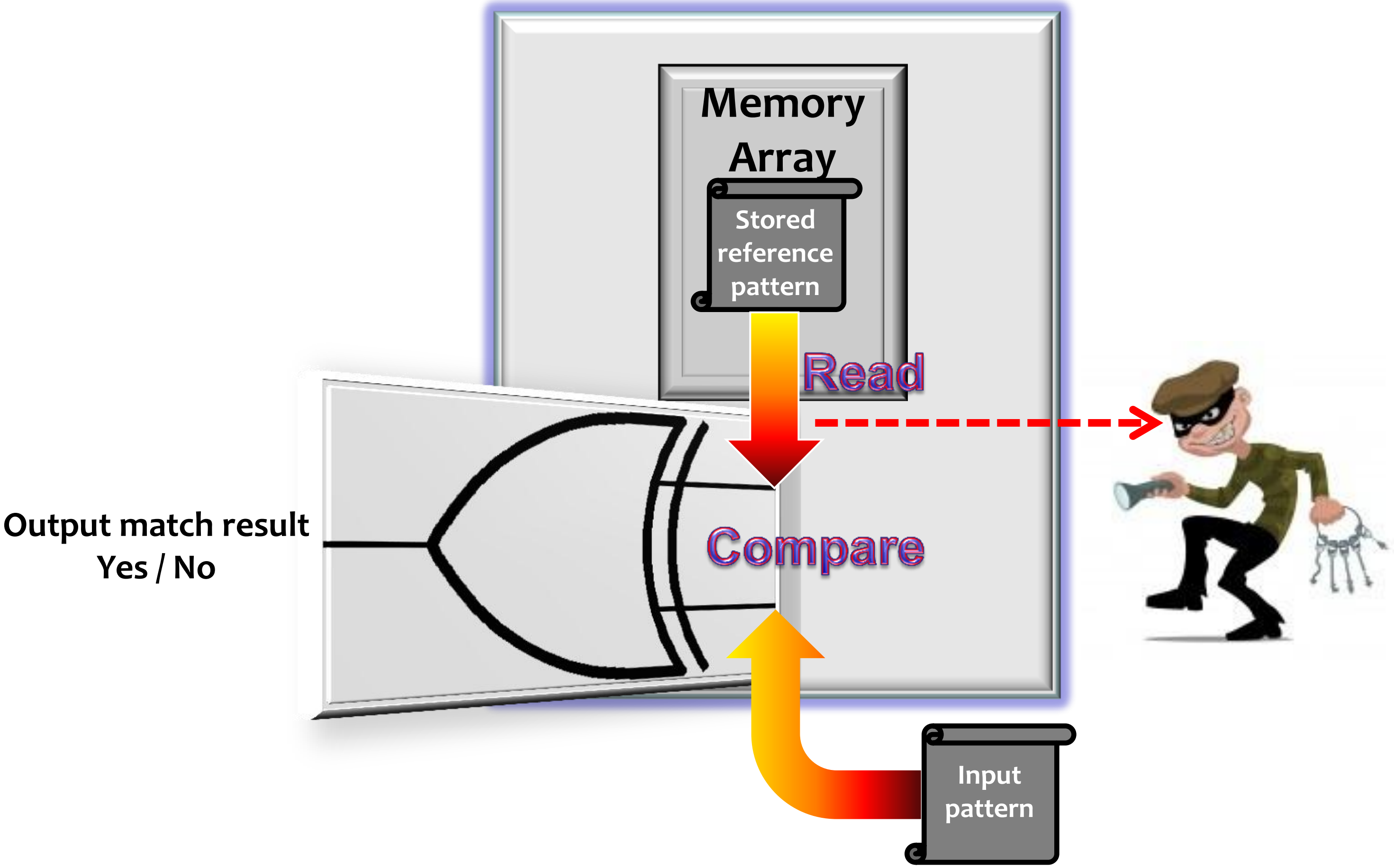


Traditional

“Read & Compare” Authentication

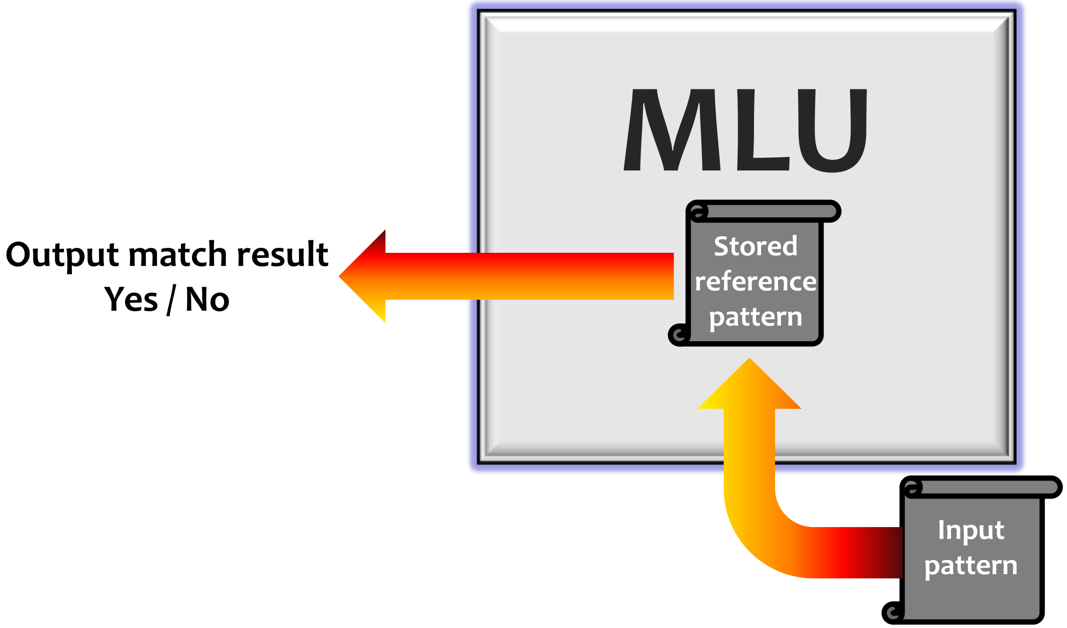


The Issue in Traditional
“Read & Compare” Authentication



Direct Match in Place

Authentication

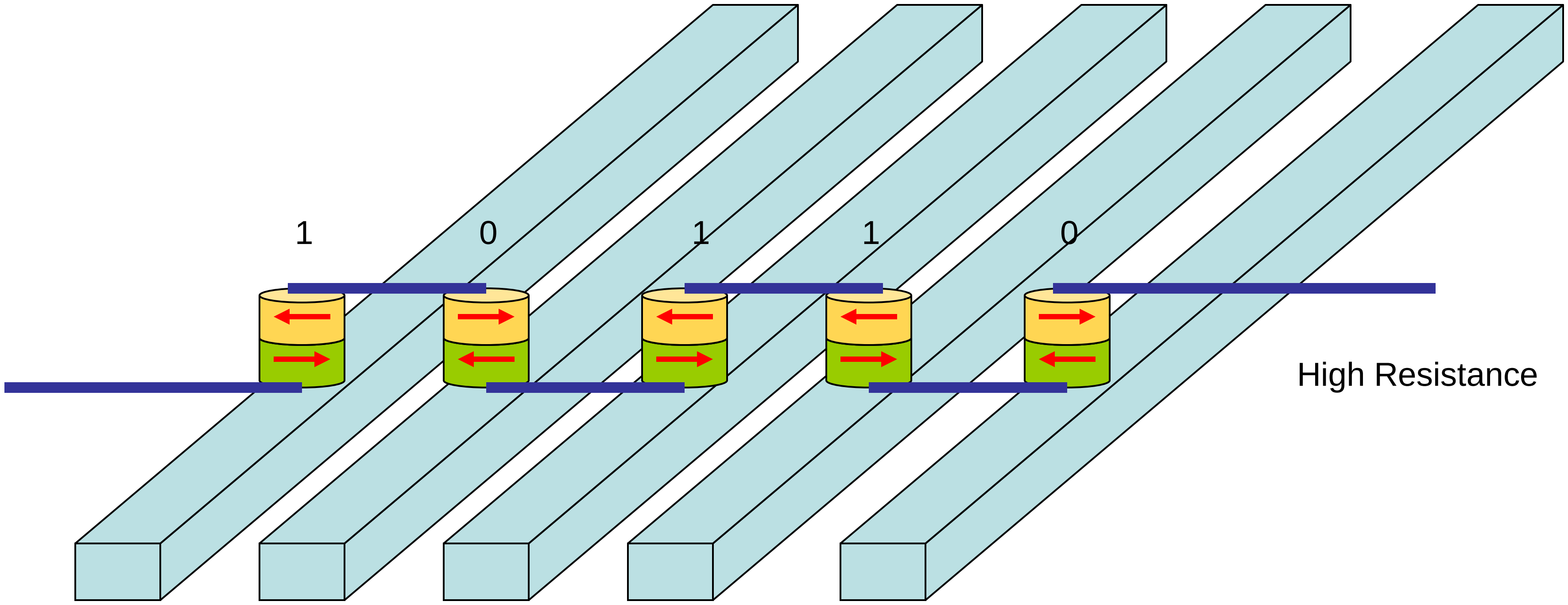


The MLU does two things: store and compare, and does it fast (15ns).

The confidential reference pattern gets compared inside the MLU.

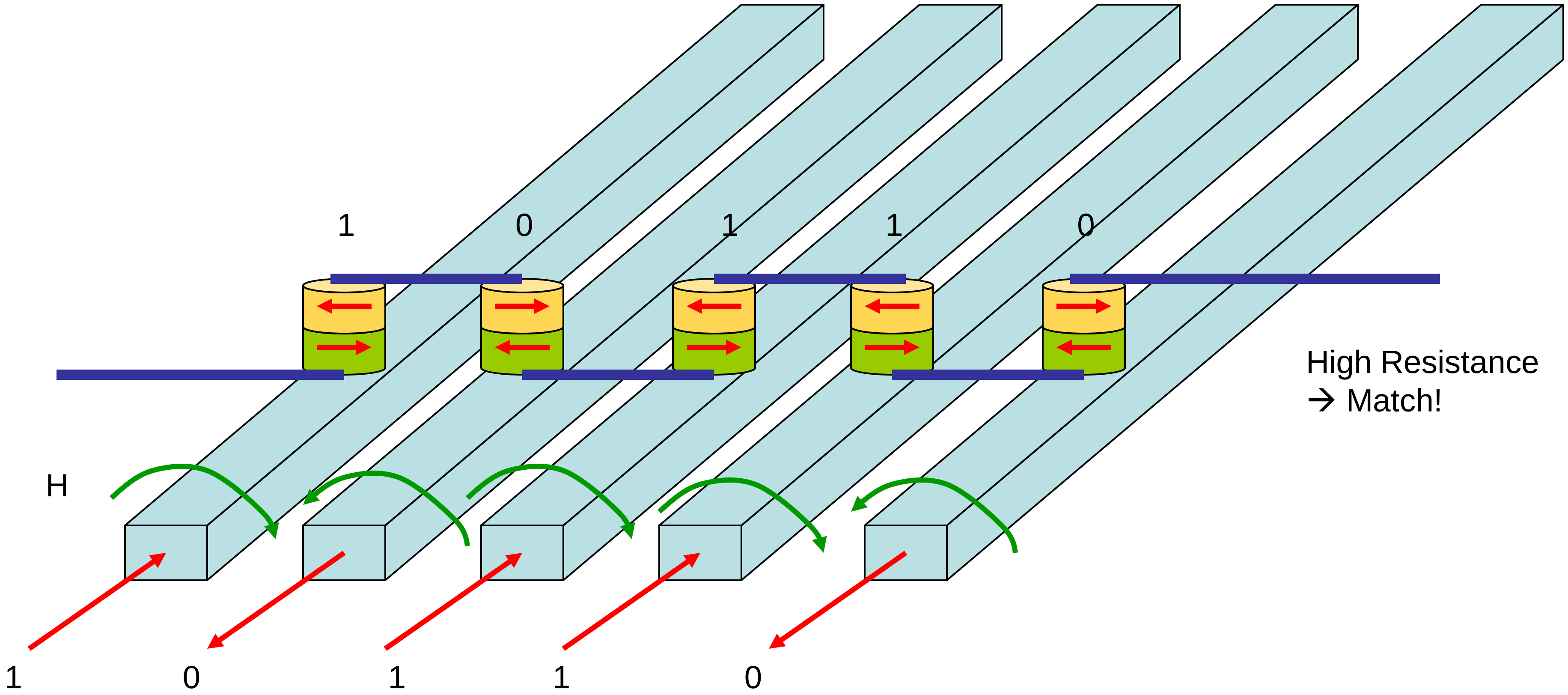
Confidential stored information never leaves the MLU.

Illustration of match chain



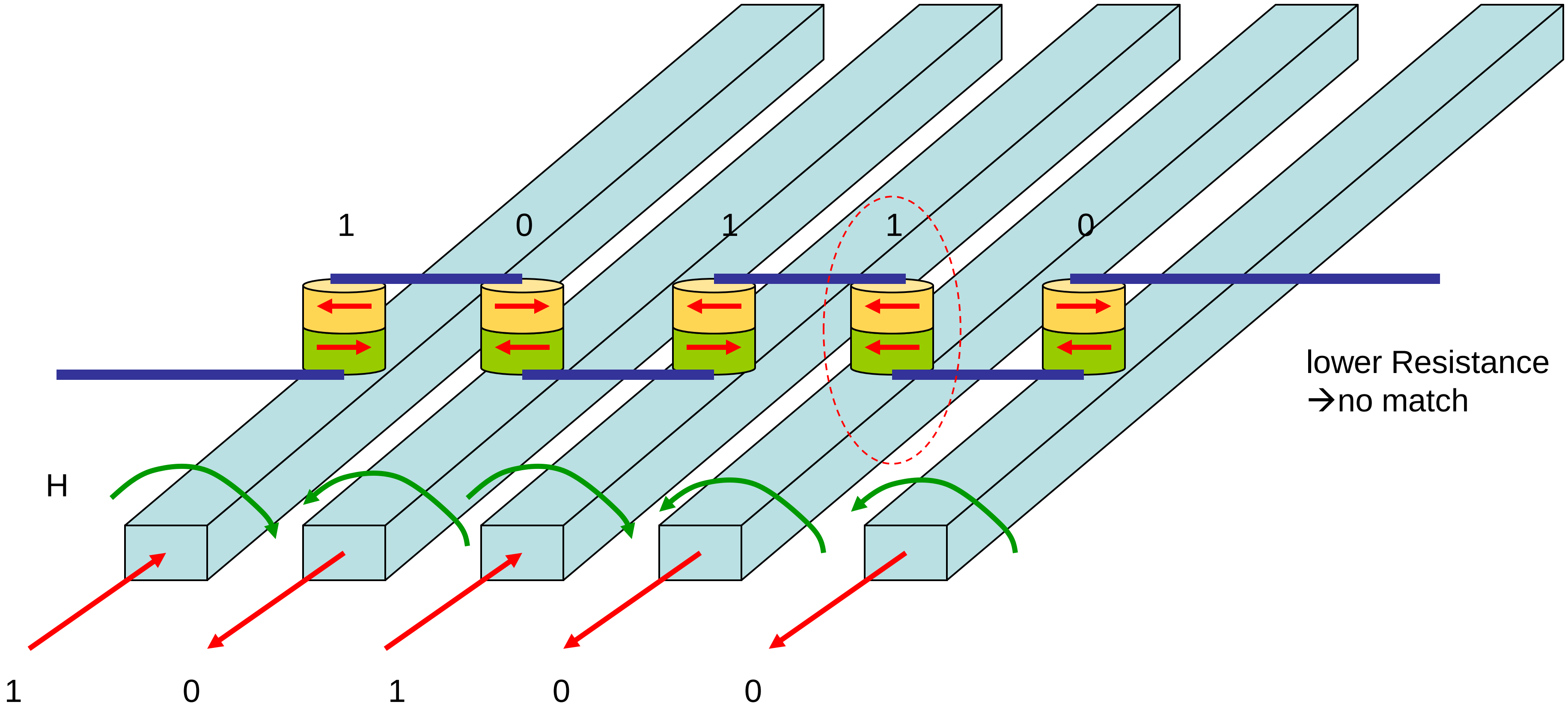
No input data

Illustration of match chain



Correct input data

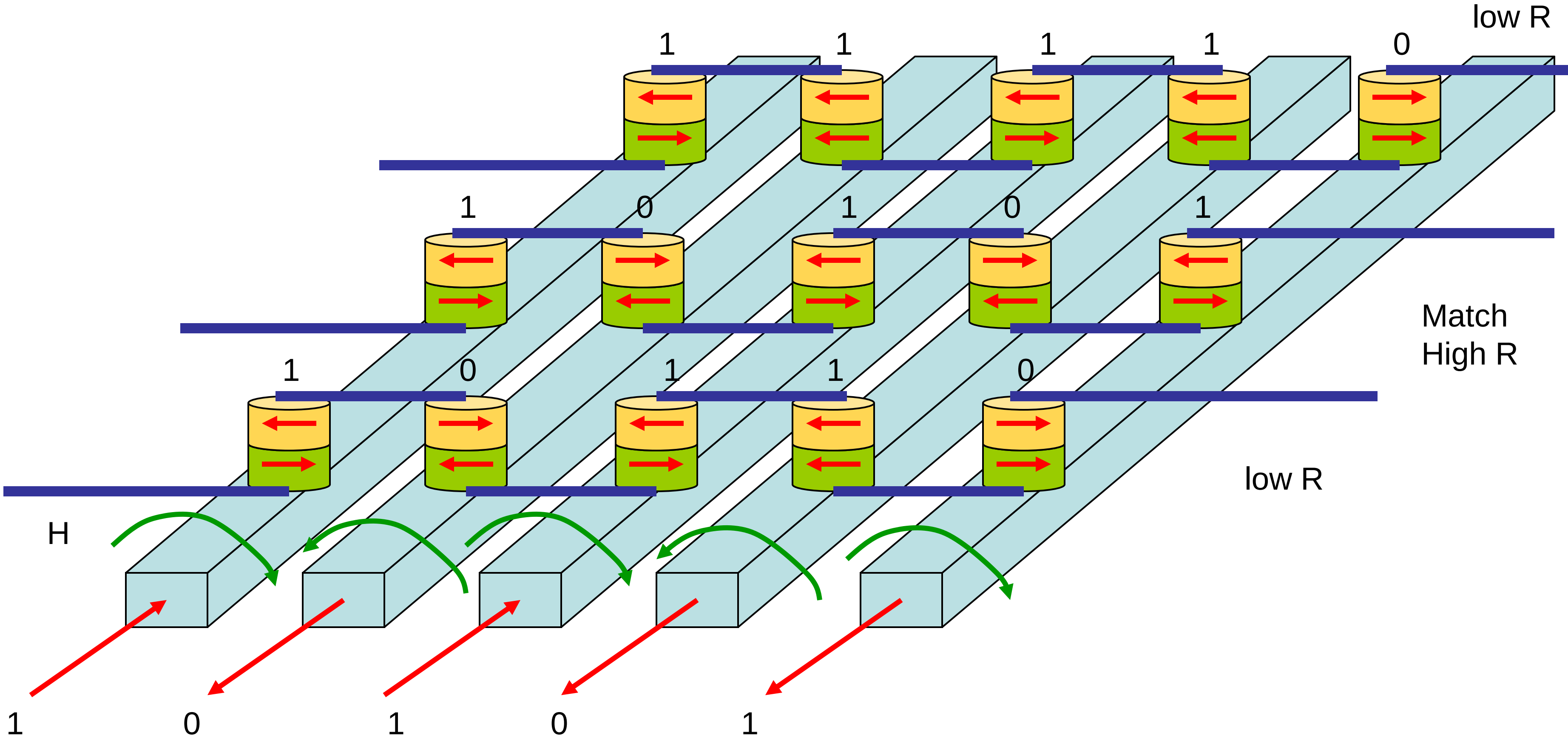
Illustration of match chain



lower Resistance
→no match

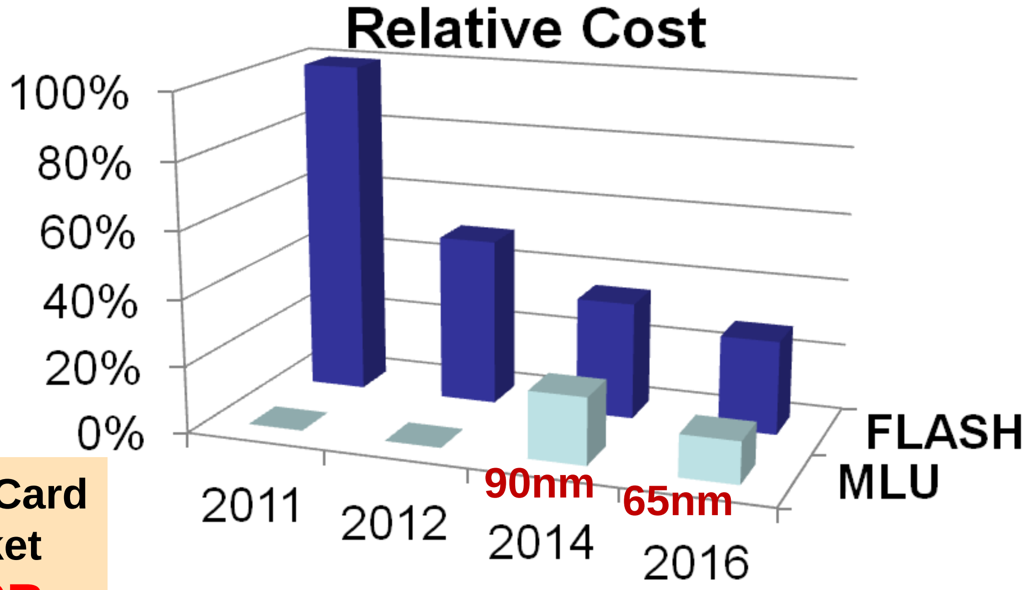
Wrong input data

search



search input data

MLU Application:
Smartcard



Smart Card Market
>$6B

MLU Advantages:

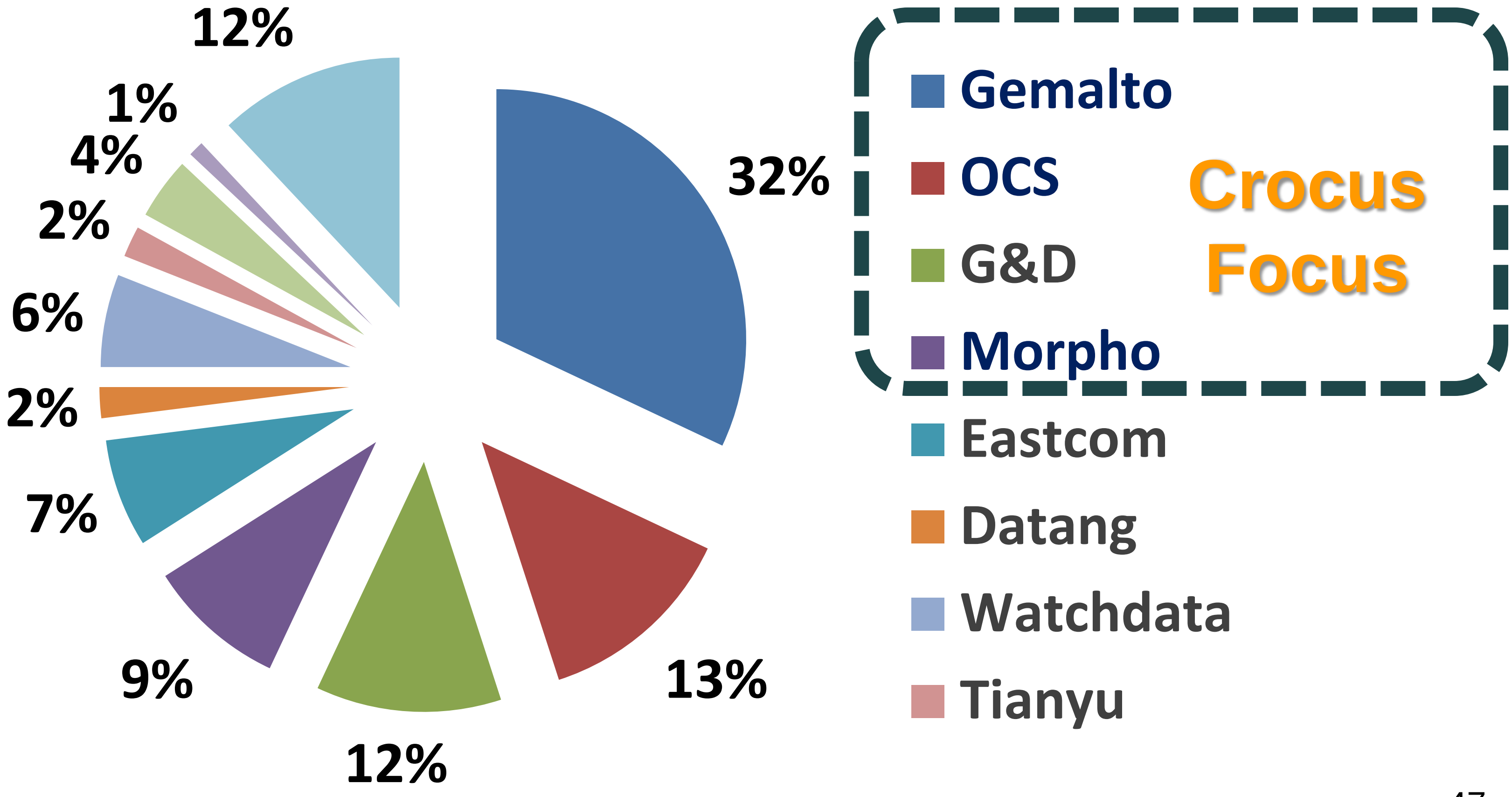
- **Sustainable Lower Cost …………**2 Masks, Low Voltage, Faster Test
- **Advanced Security Features……**Tamper Resistance, "Zero Knowledge Proof"
- **Streamlined Process Integration….**Backend Wafer Process, Standard CMOS

Need Higher protection:

Secure chip based authentication is gaining acceptance

1- Highly Secure
2- User friendly
3- Mature technology
4- Low cost

Smartcard Suppliers:



2010 all market segments

Crocus Focus

MLU Implementation

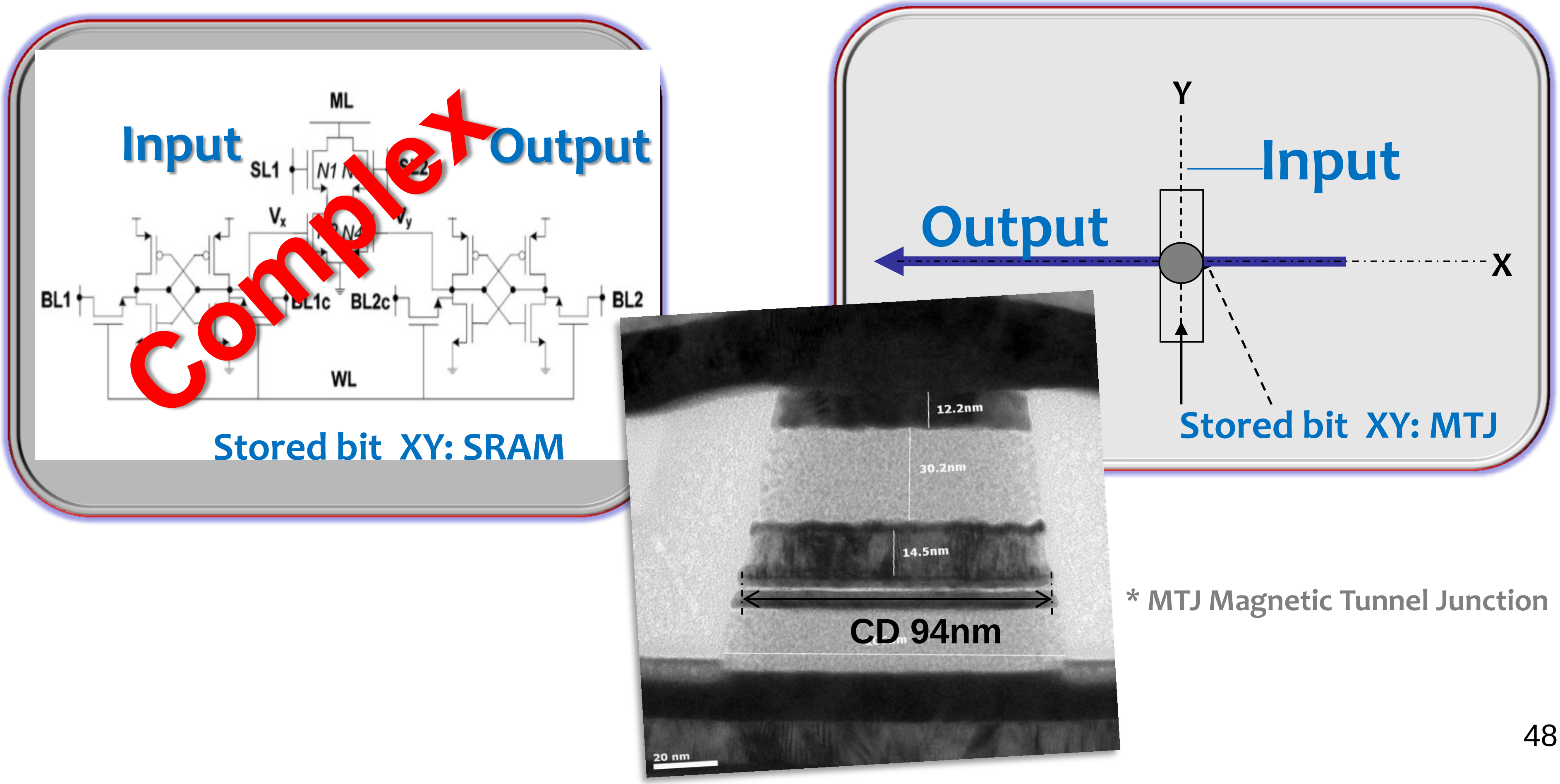
50x simpler

CMOS - CAM:

20 transistors per cell

MLU cell:

1 MTJ* per cell



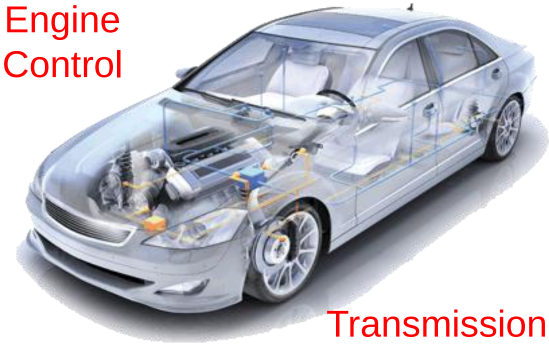
* MTJ Magnetic Tunnel Junction

MLU Application:

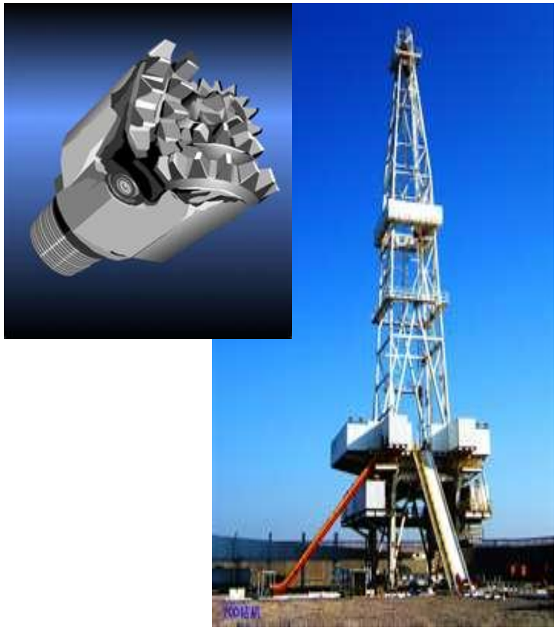
High Temperature & Sensor

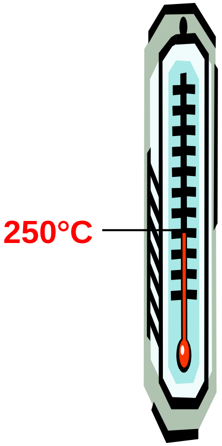
Automotive is one of the fastest growing segments of the semiconductor market

$23B in 2011



Oil drilling & Industrial is niche volume but high value





MLU Advantages:

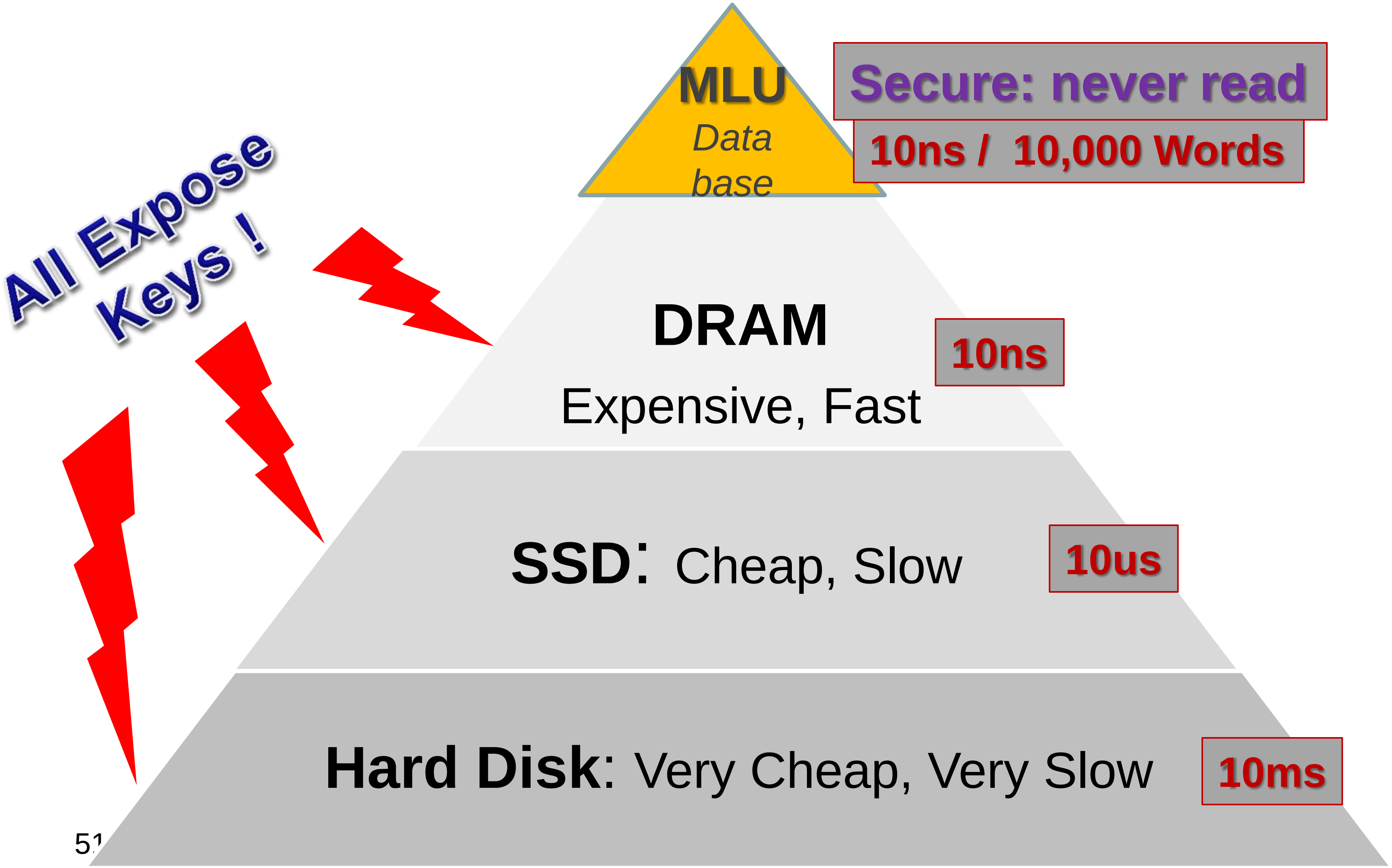
- **Capable of 250°C operation…**MLU data storage at very high temperatures
- **Sustainable Lower Cost ……..**2 Masks, Low Voltage, Faster Test
- **High Sensitivity ……………….**> 10^4 field range, Integration with CMOS

MIP Signature data base

Check only - Non readable

MLU Signature
Data base

Positioning MLU in the Cloud:
Random access



All Expose Keys !

MLU
Data base

Secure: never read

10ns / 10,000 Words

DRAM
Expensive, Fast

10ns

SSD: Cheap, Slow

10us

Hard Disk: Very Cheap, Very Slow

10ms

Product development work

- Secure Bio-metric chip for terminals
- Bio-metric data base for search for GSPS engines
- Irreversible NV-memory loss modes
- Image recognition
- Look up table for CPU HW acceleration
- …

Acknowledgements

Crocus' Technical team

France: Magnetic physics & security

California: Microelectronic team & design

Crocus' R&D partners

LETI/CEA, Spintec, SVTC and Tower , IBM

Question?